SFF-8636

Specification for

Management Interface for Cabled Environments

Rev 2.9 April 21st, 2017

Secretariat: SFF TA TWG

Abstract: This specification defines a common management interface for 4-lane pluggable transceiver modules, direct attach modules and shielded cable assemblies. Physical layer and mechanical details of the connector interface are outside the scope of this document.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review at http://www.snia.org/sff/specifications and written comments are solicited from readers via http://www.snia.org/feedback. Comments received by the members will be considered for inclusion in future revisions of this specification.

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Change History:

Rev 0.9
- Clarified wording in 6.2.2

Rev 1.0
- Added missing reservation entries (Bytes 133, 134, and 220). Modified bit entry labels (Bytes 93 and 136).

Rev 1.2
- Editorial: Formatted Word controls to improve pagination breaks and comply with style guide.

Rev 1.3
- Table 20 Identifier Values and Table 24 Encoding Values modified to point to SFF-8024 as the reference for later values and codes.

Rev 1.4
- Added Revision Compliance Byte. Changed Bytes 1, 131, 138, 146, 164, 188, and 189 to comply with latest SFF-8436 map. Added 12 Gbps SAS bit in Byte 133. Various grammatical changes made.

Rev 1.5
- Added functionality for QSFP28 (4x25G, 4x28G) transceivers per the requirements of 100GE, EDR Infiniband and 128GFC Fibre Channel. Tables 7, 8, 10, 12, 13, 17, 19, 20, 21, 23, 29, 29A, 32A, 36, 37, 41 and section 6.2.5, 6.3.6, 6.3.12, 6.3.27.

Rev 1.6
- Abstract and Scope corrected to include transceiver modules as well as shielded cables as intended applications.

Rev 1.7
- Editorial: Expanded 2.1 to include specifications referenced in the body. Near-invisible superscripts were modified to be visible text and cross-references made dynamic.
- Reference to SFF-8078 in Table 13 Control Function Bytes corrected to SFF-8079.
- Table 20 Identifier Values and Table 24 Encoding Values which had been retained in the text for information were removed.
- Table 23 Specification Compliance and Table 29A Extended Ethernet Compliance Codes tables were moved to SFF-8024.

Rev 1.9
- Clarified Address 5 Loss of Lock indicators as latched
- Added Address 93 bit 2 High Power Class Enable lockout feature
- Clarified Address 98 CDR controls as 1b=On and 0b=Off (ie. bypassed)
- Clarified Table 21 for Address 129 bits 1-0 to refer to Address 93 bit 2
- Added Adaptive EQ indicator in Address 193 bit 3.
- Clarified Address 194 bits 7-6 setting as 1b=Controllable, 0b=Fixed
- Added Address 220 bit 2 to identify Tx Power diagnostic monitoring supported
- Added Page 03h Address 224 to define magnitude of Tx EQ and Rx Emph supported
- Added TX Adaptive EQ capability indicator, Page 00h, Address 193 bit 3
- Added TX Adaptive EQ (per ch) control bits in Page 03h, Address 241 bits 3-0
- Added TX Adaptive EQ Fault flag in Address 6 and masking bits in Address 101
- Added RX output amplitude support indicators in Page 03h Byte 225
- Added text to section 6.3.2 indicating that the power class identifiers specify worst case maximum power dissipation.
- Added Initialization complete flag to Byte 6 bit 0.

Rev 2.0
- Changed the amplitude setting 0 from 200-400 to 100-400mv.
- Added Version 2 to address 141.
- Added Version 2 Rate Select table to Table 14 with: 00 as under 12Gb/s, 01 as between 12Gb/s and 24Gb/s, 10 as between 24Gb/s and 26Gb/s and 11 is above 26Gb/s
- Changed revision register compliance bit for revision 1.9 to 2.0 (1.9 was never released)
- Editorial changes to fix spelling and maintain consistent naming.

Rev 2.1
- Assigned Page 00h Bytes 111-112 for use by PCI-SIG
- Restored Table 23 and Table 24 from SFF-8024
- Replaced 'See SFF-8024 Table 4-x' with 'See SFF-8024 Transceiver Management'
- Made Page/Address Byte, Page/Address, Page/Byte synonyms common: as Page/Byte
- Added Page/Byte/Bit location to those table titles which did not have it
- Alphabetized abbreviations and added some that were missing
- Deleted 'Ethernet' in respect to Extended Specification Compliance Codes
- Replaced Figure 13 with current use of memory
- Other minor corrections e.g. added 'h' as in Page 00h when it was missing

Rev 2.2- During the review of Rev 2.1 it was recommended that:
  o the contents of Table 22 Connector Type be moved to SFF-8024.
  o the contents of Table 24 Encoding Values be returned to SFF-8024.
- Other minor editing improvements

Rev 2.3
- Nomenclature of 10e in Section 2.5 Abbreviations replaced by 10^

Rev 2.4
- Adopted Figure/Table numbering style of current template
- To make correlation of previous Change History easier for readers, a Cross Reference of Figures and Tables was prepared.

Rev 2.5
- Table 6-30 split creating new Table 6-31. Old Tables 6-31 to 6-35 become new Tables 6-32 to 6-36.
- Figure 1-1 updated to reference SFF-8665 (QSFP28)
- 2.1 Industry Documents - added SFF-8665
- Table 5-3 updated to include Bytes 93, 98, 99 and 107
- Table 5-6 updated to include sub-headings with page numbers and to add Bytes 94-97, 100-104, 105-106, 111-112, 114-118. Changed description of Page 03h Bytes 226-241 to Optional Channel Controls. Added Page 03h Bytes 254-255.
- 6.1 Overview. Added fourth paragraph explaining details of non-implemented pages.
- Figure 6-1. Updated Page 00h descriptions for Bytes 22-33, 100-104, 105-106, 108-110, 111-112, 113 and 114. Removed '(Cable Assemblies)' from Page 03h sub-heading.
- 6.1.1.1 shortened column descriptions by removing 'applications' from each one.
- Table 6-1. Updated descriptions at Bytes 22-33, 86-98, 99, 100-104, 105-106, 108-110, 111-112, 113, 114-118.
- 6.2.2 Status Indicators. Added text to third sentence of first paragraph to emphasize that both the IntL pin and bit are asserted upon completion of a power up reset.
- Table 6-3. Added value 07h for rev 2.5. Added text to value 00h - 'Do not use for...'. Updated value 01h to say SFF-8436 rev 4.8 or earlier.
- Table 6-5. Additional description for Byte 6 bit 0 Initialization Complete Flag referencing Table 6-25 for the new Initialization Complete Implemented bit.
- 6.2.4 Free Side Device Monitors. Added fifth paragraph to explain placement of temperature sensor.
- Table 6-8. Added Bytes 66-73 description for reserved channel monitor set 5.
- Table 6-13. Corrected Byte 101 bits 7-4 names from L-Tx… to M-Tx…
- 6.2.9 Free Side Device Properties. Added paragraphs 5 and 6 to explain the purpose of Byte 113 bits 3-0 and Byte 113 bits 6-4. This byte is added for breakout cables.
- Table 6-14. Added Byte 113 bits 6-4 Far End Implementation and bits 3-0 Near End Implementation descriptions.
- 6.2.11 Page Select. Added last sentence to define behavior when the host writes an unsupported page value.
- Table 6-15. Removed sub-headers for Base ID, Extended ID and Vendor Specific ID Fields. Changed Name of Byte 130 from 'Connector, Media' to 'Connector Type'. Updated description of Byte 146 to clarify that all cable assemblies are in units of 1m and OM4 fiber lengths are in units of 2m.

- 6.3.8 through 6.3.12. Added words to clarify usage for separable modules and for cable assemblies.
- 6.3.13. Additional sentence referencing Byte 130 (connector type) to distinguish active optical cable (AOC) from separable module (SM).
- Table 6-20. Added '/ Undefined' to value 1000b.
- 6.3.27 Diagnostic Monitoring Type. Added additional words to fourth and fifth paragraphs to explain the treatment of Byte 220 bits 3-2 when not set.
- Table 6-25. Added Byte 221 bit 4 Initialization Complete Flag Implemented, with explanation.
- Table 6-29. Reformatted with # Bytes column and updated descriptions.
- Table 6-31. Added Byte 225 bits 5-4 Rx output emphasis type with description.
- Table 6-32. Bytes 226-233 from Vendor Specific to Reserved. Added descriptions for Byte 241 bits 3-0 to specify that adaptive equalization is the default if it is implemented.
- Table 6-35. Code 1xxx from Vendor Specific to Reserved.
- 6.6.2 Optional Channel Controls. Added 2 sentences at the end of first paragraph to explain that free side devices can limit the maximum emphasis supported using Byte 224.

Rev 2.6
- Title changed per request to comply with the lexicon
- Table 5-4 and other content consolidated into Table 5-3.

Rev 2.7
- Updates as per “bucket list” comment resolution.
- Editorial corrections throughout.
- Added SAS 24.0 Gbps bit in Table 6-17.

Rev 2.8.1
- Cover Page: added David Lewis to Points of Contact.
- Expressions of Support by Manufacturers: Removed names pending new ballot.
- Cross Reference of Figures and Tables: Added new Table 6-10 and incremented all Table numbers from 6-11 to 6-37
- 2.1 Industry Documents: added SFF-8436, INF-8438, SFF-8679.
- Figure 6-1 Common Memory Map: changed description of bytes 100-104 to match other places in the document.
- Table 6-2 Status Indicators: Byte 2, bits 7-4 now reserved for microQSFP MSA module state field. Improved descriptions for byte 2 bits 1-0.
- Table 6-3 Revision Compliance: Added 08h for SFF-8636 Rev 2.8.
- Table 6-5 Free Side Monitor Interrupt Flags: Added byte 6, bit 1 for TEC readiness flag.
- Table 6-9 Control Function Bytes: New descriptions for Byte 93, bit 2-0.
- 6.2.6 Control Functions: 4 new paragraphs describing power levels and related control functions. New Table 6-10 Truth Table for Enabling Power Classes. All following table numbers increased by 1.
- 6.2.7.2 Extended Rate Selection: Modified first sentence to clarify that page 00h, byte 195 bit 5 needs to be set for rate selection to be supported.
- Table 6-14 Hardware Interrupt Pin Masking Bits: Added byte 103, bit 1 for TEC readiness flag masking bit.
- Table 6-15 Free-Side Device Properties: Byte 114 removed from reserved and assigned for microQSFP MSA maximum duration fields.
- Table 6-16 Upper Page 00h Memory Map: Added definition to byte 142 Length (SMF) to say that a value of 1 shall be used for reaches from 0 to 1 km. Added a new use for byte 145 Length (OM1 62.5 um) or Copper Cable Attenuation. Corrected byte 189 copper cable attenuation frequency from 12 to 12.9 GHz.
- Table 6-19 Extended Rate Select Compliance Tag Assignment: Modified description of byte 141 bits 1-0.
- 6.3.11 Length (OM1) or Copper Cable Attenuation: Added new paragraph describing support for copper cable assemblies.
- Table 6-22 Extended Module Code Values: Added byte 164 bit 5 for HDR module code.
- 6.3.20: corrected section title to Wavelength Tolerance or Copper Cable

Attenuation.
- Table 6-23 Option Values: Byte 195 bit 0 used to indicate support for pages 20h-21h.
- Table 6-25 Diagnostic Monitoring Type: Added byte 220 bits 5-4 to indicate support for temperature and supply voltage monitoring.
- Table 6-26 Enhanced Options: Added byte 221 bit 1 for TEC readiness flag implemented.
- 6.6 Upper page 03h: first paragraph modified to say that page 03h includes ability registers for optional equalizer, emphasis and amplitude.
- 6.6.1 Free-Side Device and Channel Thresholds: Added paragraph after Table 6-31.
- Table 6-33 Optional Channel Controls: Added byte 228 Maximum TEC stabilization time and byte 229 Maximum CTLE settling time. Improved descriptions for bytes 238-239 Rx Output Amplitude Controls.
- 6.6.3 Optional Channel Controls: Added paragraph after Table 6-36 to clarify that Rx amplitude and emphasis are measured at the relevant test point.
- Added new section 6.7 for Tables 20h-21h.
- Added Annex A – alternative text for section 6.2.7 Rate Select and Configuration for Multi-Rate Modules.

Rev 2.8.2
- Table 5-3 Added pages 20-21h
- Figure 6-1 Replaced with new figure that includes pages 20-21h
- Table 6-2 Replaced (O) with (-) in byte 2 bits 7-4
- Table 6-2 Removed (if pin supported) from description of IntL bit
- Table 6-2 Made the IntL bit (R) for all free side devices
- Table 6-5 Updated the description of TC readiness flag to reflect correct reassert behavior
- 6.2.4 Removed reference to an external temperature control location
- Table 6-9 Changed all entries from (O) to (-) for PC free side device
- Table 6-15 Updated descriptions of Advanced Low Power bits and Min. Operating Voltage bits
- Table 6-15 Provided names of PCI SIG specifications that use bytes 111-112
- Table 6-16 Updated descriptions of bytes 142-146 to say that the link lengths apply at the stated bit rate
- Table 6-23 Changed byte 193 bit 4 from reserved to “Tx Input Adaptive Equalizer Freeze Capable” bit.
- Table 6-32 Moved Max. TC Stabilization Time and Max. CTLE Settling Time bytes from Table 6-33 to end of Table 6-32. Added units to descriptions. Changed table title to include timing.
- Table 6-33 Changed byte 233 bits 4-0 from reserved to Tx Adaptive Equalizer Freeze control bits.
- Section 6.7 Reorganization and rewording throughout.

Rev 2.8.3
- Editorial changes for bucket list items that were missed in rev 2.8.2

Rev 2.9
- Published version incorporating editorial comments received during approval ballot.

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants. Material presented to SFF becomes public domain, and there are no restrictions on the open mailing of the presented material by Members.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:

http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

http://www.snia.org/sff/specifications See Doc #: SFF-8000

If you wish to know more about the SFF TWG, the principles which guide the activities can be found at:

http://www.snia.org/sff/specifications See Doc #: SFF-8032

Suggestions for improvement of this specification will be welcome, they should be submitted to:

http://www.snia.org/feedback

CONTENTS

FIGURES

TABLES

1 Scope

This specification defines a common memory map and protocol that can be used to manage both 4-channel pluggable transceiver modules and 4-channel managed external cable interface implementations. Physical layer and mechanical details of the interface are outside the scope of this document. Memory map details and communication protocol used to transfer the information are described within this document. This approach facilitates a common memory map and management interface for applications with different mechanical, physical layer and otherwise different implementations. For example, SFF-8449 defines a 4-channel solution which documents the management interface physical layer, references SFF-8636 to ensure compatibility with the common memory map and protocol.

This specification does not apply to the CFP MSA family of modules, which use the MDIO interface and a different memory map.

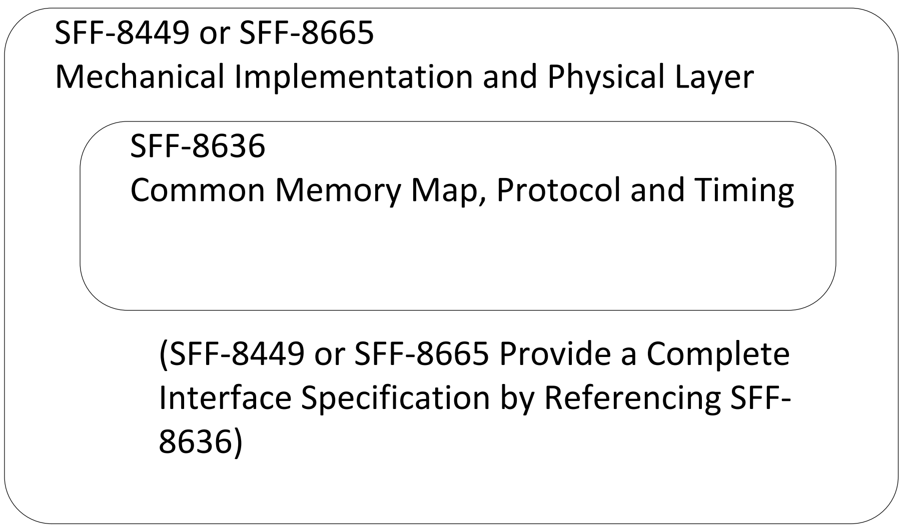

FIGURE 1-1 HIERARCHY OF INTERFACE SPECIFICATIONS (EXAMPLE)

1.1 Copyright

granted if the Exception request is not acknowledged within ten (10) business days of SNIA's receipt. Any denial of permission for the Exception shall include an explanation of such refusal.

1.2 Disclaimer

The information contained in this publication is subject to change without notice. The SNIA makes no warranty of any kind with regard to this specification, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this specification.

Suggestions for revisions should be directed to http://www.snia.org/feedback

2 References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification. They can be downloaded from http://www.snia.org/sff/specifications.

- SFF-8024 SFF Committee Cross Reference to Industry Products
- INF-8074 SFP (Small Formfactor Pluggable) 1 Gb/s Transceiver
- SFF-8079 SFP Rate and Application Selection
- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface
- SFF-8436 QSFP+ 10 Gbs 4X Pluggable Transceiver
- INF-8438 QSFP (Quad Small Formfactor Pluggable) Transceiver
- SFF-8449 Shielded Cables Management Interface for SAS
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8679 QSFP+ 4X Base Electrical Specification

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on are listed in http://www.snia.org/sff/specifications See Doc #: SFF-8000.

2.3 Conventions

The English convention of numbering is used (i.e., a comma separates the thousands and higher multiples, and a period is used as the decimal point). This is equivalent to the ISO/IEC convention of a space and comma.

English	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Abbreviations

For the purpose of this SFF Specification the following units and abbreviations apply:

AC	Active Cable
AO	Active Optical cable
b	binary (suffix to preceding binary based number)
C	degrees Celsius (thermal unit associated with a value)
C	Conditional upon another parameter which is optional
dB	decibel (base 10 logarithmic unit)
dBm	decibels above one milliwatt (i.e., 10dBm)
Gbps	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)
h	hexadecimal (suffix to preceding hexadecimal based number)
Hz	hertz (i.e., cycles per second)
kHz	kilohertz (i.e., 10^3 cycles per second)
km	kilometer (i.e., 10^3 meters)
LSB	Least Significant Bit
m	meter (unit of length)
mA	milliampere (i.e., 10^-3 amperes)
Mbps	megabits per second (i.e., 10^6 bits per second)
MHz	megahertz (i.e., 10^6 cycles per second)
ms	millisecond (i.e., 10^-3 seconds)
MSB	Most Significant Bit
mV	millivolt (i.e., 10^-3 volts)
mW	milliwatt (i.e., 10^-3 watts)
nm	nanometer (i.e., 10^-9 meters)
ns	nanosecond (i.e., 10^-9 seconds)
O	Optional
P-P	peak-to-peak
PAM4	Four-level pulse amplitude modulation
PC	Passive Cable
ps	picosecond (i.e., 10^-12 seconds)
R	Required
s	second (unit of time)
SM	Separable Module
TC	Temperature Controller (e.g. thermo-electric cooler)
uA	microampere (i.e., 10^-6 amperes)
um	micrometer (i.e., 10^-6 meters)
us	microsecond (i.e., 10^-6 seconds)
uV	microvolt (i.e., 10^-6 volts)
uW	microwatt (i.e., 10^-6 watts)
V	volt (unit of electrical potential)
W	watt (unit of electrical power)

<table>
<tr><td colspan="8"></td><td>MSB</td><td colspan="6">8-bit Field</td><td>LSB</td></tr>
<tr><td>MSB</td><td colspan="14">16-bit Field</td><td>LSB</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

3 Definitions

3.1 Fixed versus Free

3.1.1 Fixed

The terminology "fixed" is used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". Other terms commonly used are "female" and "socket connector". The term "fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the fixed end of a connection, for example, on the board or bulkhead side.

3.1.2 Free

The terminology "free" is used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". Other terms commonly used are "male" and "pin connector". The term "free" is adopted from EIA standard terminology as the gender that most commonly exists on the free end of a connection, for example, on the cable side.

3.2 Passive Cable

In this specification, a passive cable only requires power to operate the management interface circuitry.

3.3 Active Cable

In this specification, an active cable requires power for circuitry that is integral to any of the TX/RX high speed serial channels supported by the cable. In addition, the active cable requires power to operate the management interface.

3.4 Pluggable Transceiver Module

In this specification, a pluggable transceiver module requires power for the management interface and for the circuitry integral to the TX/RX high speed serial channels supported by the module. The module also has a media dependent interface (MDI), such as a duplex single mode fiber or a parallel multimode fiber connector. The high speed electrical interface of the module may contain equalizers and retimers (CDRs) which are managed by registers defined in this management interface specification.

4 General Description

The common management interface provides a method for the fixed side to determine the characteristics and status of the free side. In some implementations, the interface also provides a mechanism to control the operation of the free side circuitry. For the case where the free side is a cable, the fixed side can determine if the cable is passive, active copper, or active optical. For the case where the free side is a transceiver module, the fixed side can determine if the module is single mode, multimode or copper and which transmission standards are supported. Parameters such as supplier, part number, propagation delay and loss (for passive cables) can also be determined.

4.1 Fixed-to-Free Side Block Diagram

Note, in Figure 4-1, the limitations in scope of SFF-8636 in the fixed-to-free side management interface.

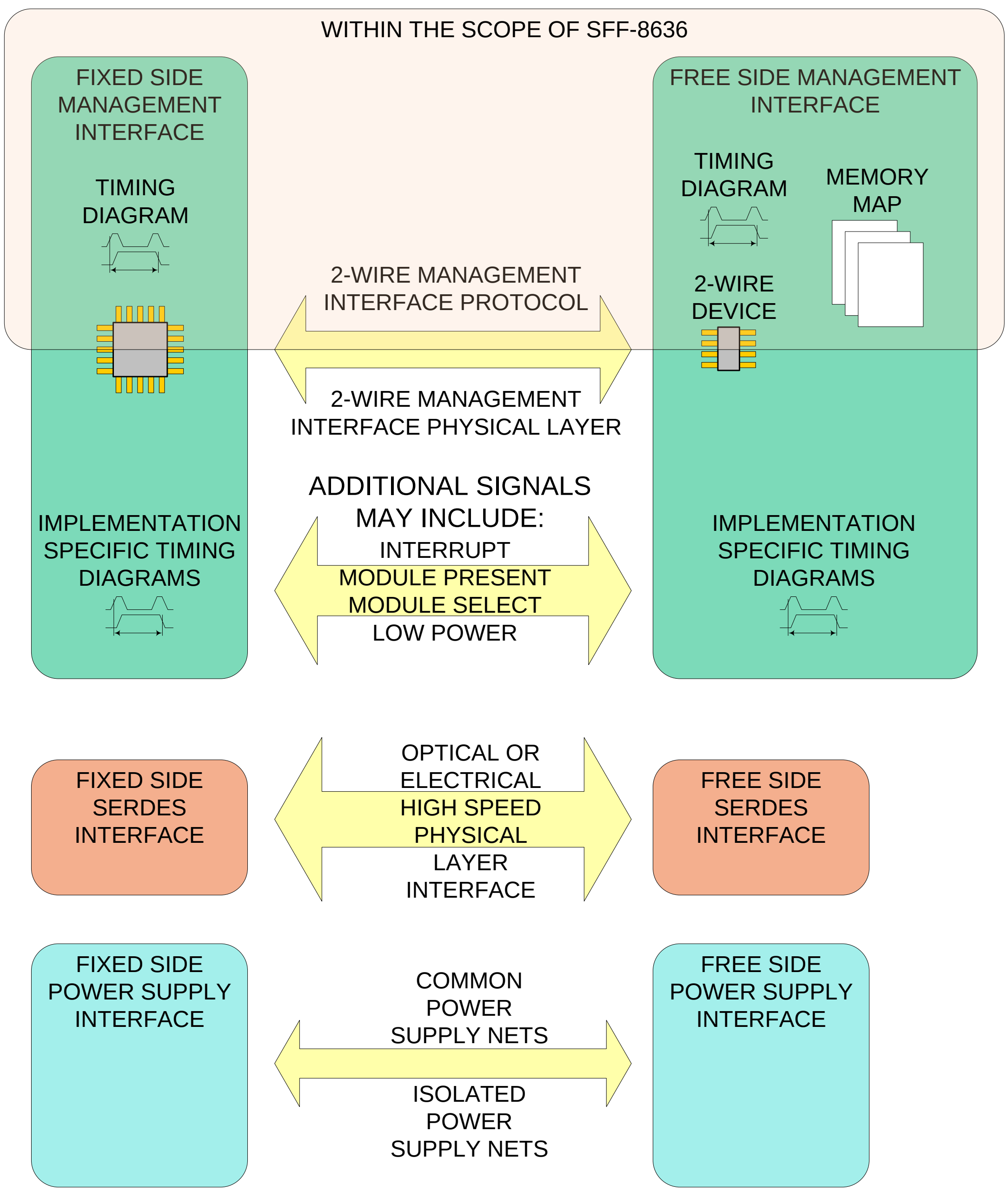

FIGURE 4-1 COMMON MANAGEMENT INTERFACE BLOCK DIAGRAM

4.2 Signal Definition

The 2-wire management interface shall include the following physical layer signals.

4.2.1 SCL

2-wire interface clock.

4.2.2 SDA

2-wire interface data.

4.2.3 Other Physical Layer Signals

Additional physical layer signals such as power, module present, interrupt, reset and low-power mode may be implemented but are beyond the scope of SFF-8636. Memory map parameters may reference physical layer signals other than SCL and SDA to reserve space but these details are beyond the scope of this specification.

4.3 Physical Cable Assembly Implementation

4.3.1 Direct Attach

The interconnect implementation may be a direct attach passive, active copper or optical cable interconnect.

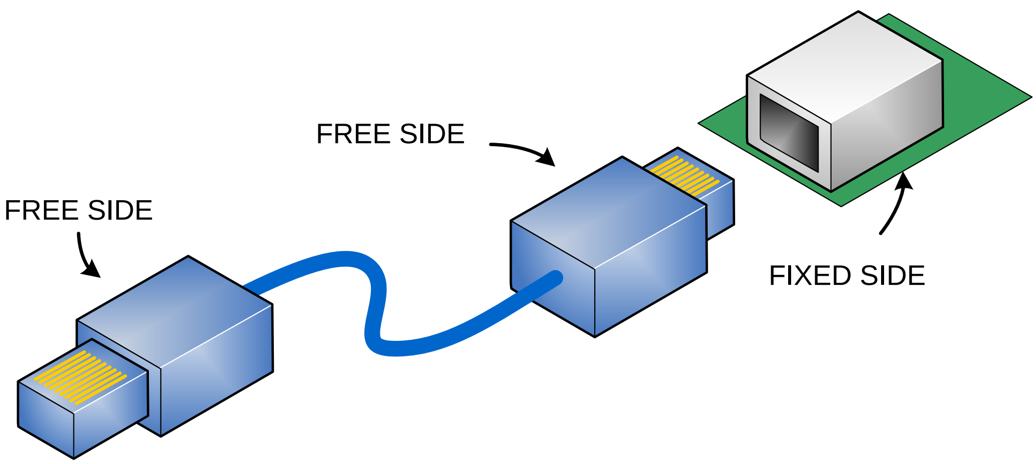

FIGURE 4-2 DIRECT ATTACH CABLE ASSEMBLY IMPLEMENTATION

4.3.2 Separable

Figure 4-3 depicts a separable active copper or optical transceiver interconnect implementation. Only the management interface between the fixed and free side is within the scope of this document.

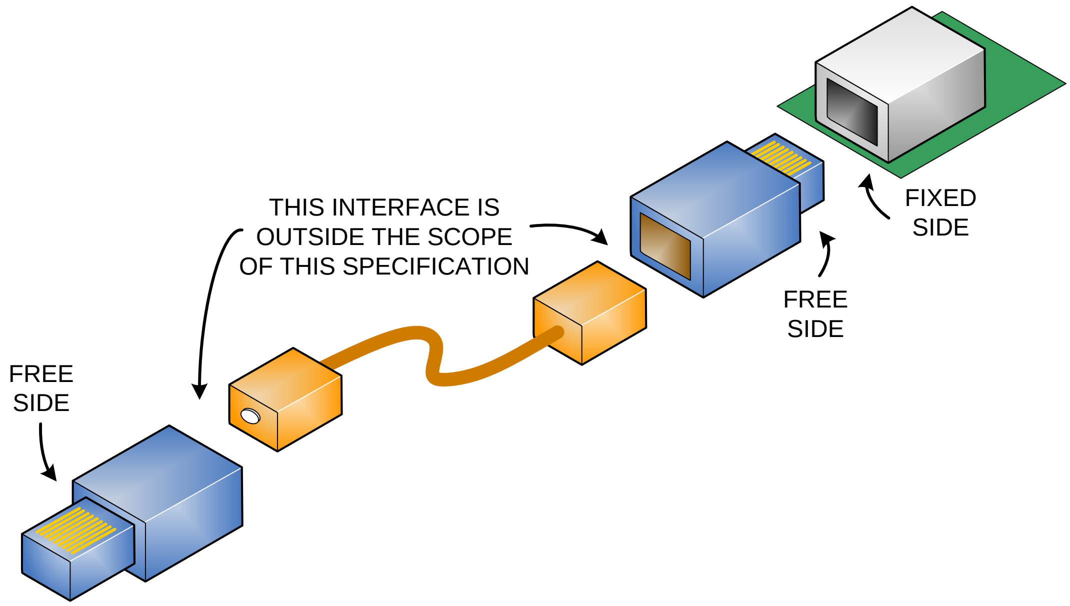

FIGURE 4-3 SEPARABLE CABLE ASSEMBLY IMPLEMENTATION

4.3.3 Management Interface Scope

The scope of the management and active cable power interfaces is limited. Note that management and power interfaces do not extend from one free side end of the cable to the other.

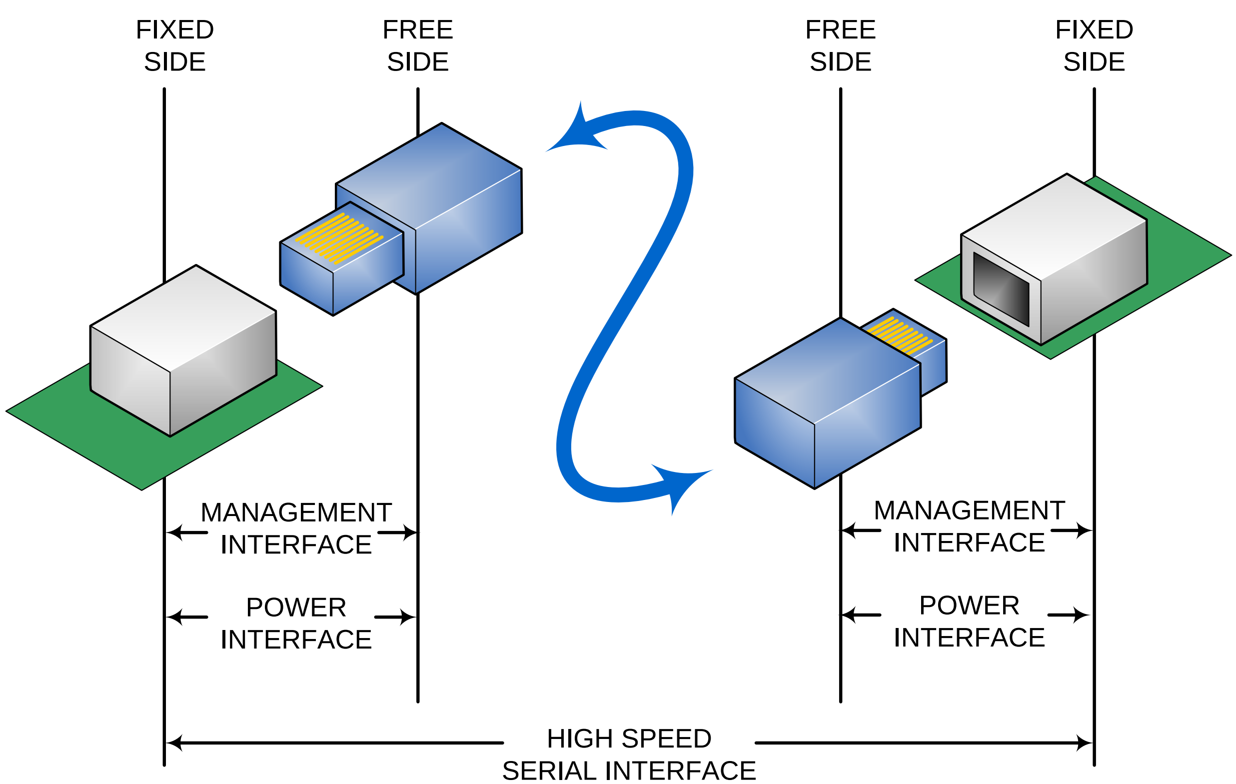

FIGURE 4-4 MANAGEMENT INTERFACE SCOPE

5 2-wire Bus Interface

5.1 Signal Interface

The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of clock (SCL) and data (SDA) signals.

The master utilizes SCL to clock data and control information on the 2-wire bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL.

The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.

5.2 2-wire Bus Protocol

5.2.1 Operational States and State Transition

5.2.1.1 Start

A high-to-low transition of SDA with SCL high is a START condition. All 2-wire bus operations shall begin with a START condition.

5.2.1.2 Stop

A low-to-high transition of SDA with SCL high is a STOP condition. All 2-wire bus operations shall end with a STOP condition

5.2.1.3 Acknowledge

After sending each 8-bit word, the side driving the 2-wire bus releases the SDA line for one bit time, during which the monitoring side of the 2-wire bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Write data operations shall be acknowledged by the slave for all bytes. Read data operations shall be acknowledged by the master for all but the final byte read, for which the master shall respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

5.2.1.4 Clock Stretching

To extend the transfer the slave asserts clock low. This can be used by the slave to delay completion of the operation.

5.2.2 Reset (Management Interface Only)

5.2.2.1 Power On Reset

The interface shall enter a reset state upon loss of power. After power is returned, the interface shall transition from the reset state within a time period that is beyond the scope of this document.

5.2.2.2 Protocol Reset

Synchronization issues may cause the master and slave state machines to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The 2-wire interface protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

a) The master shall provide up to nine SCL clock cycle (drive low, then high) to the slave
b) The master shall monitor SDA while SCL is high on each cycle.
c) If the slave releases SDA, it will be high and the master shall initiate a START operation

d) If SDA remains low after a full nine clock cycles the protocol reset has failed

5.2.2.3 Reset Signal

Some implementations may include a reset pin. If provided, upon assertion of the reset pin the free side shall transition to the reset state. The delay for the state transition is beyond the scope of this document.

5.2.3 Format

5.2.3.1 Control

After the start condition, the first 8-bit word of a 2-wire bus operation shall consist of '1010000' followed by a read/write control bit.

1	0	1	0	0	0	0	R/W
MSB							LSB

The least significant bit indicates if the operation is a data read or write. A read operation is performed if this bit is high and a write operation is executed if this bit is set low. Upon completion of the control word transmission the slave shall assert the SDA signal low to acknowledge delivery (ACK) of the control/address word.

5.2.3.2 Address and Data

Following the read/write control bit, addresses and data words are transmitted in 8-bit words. Data is transferred with the most significant bit (MSB) first.

5.3 Read/Write Operations

5.3.1 Slave Memory Address Counter (Read and Write Operations)

All 2-wire slaves maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the slave. This address remains valid between operations as long as power to the slave is maintained. Upon loss of power to or reset of the free side device, the slave address counter contents may be indeterminate. The address roll-over during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

5.3.2 Write Operations (BYTE Write)

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement. Upon receipt of this address, the slave shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the slave shall output a zero (ACK) and the master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the 2-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the slave enters an internally timed write cycle, tWR, to internal memory. The slave disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the internal memory write is complete.

Note that 2-wire interface 'Combined Format' using repeated START conditions is not supported on write commands.

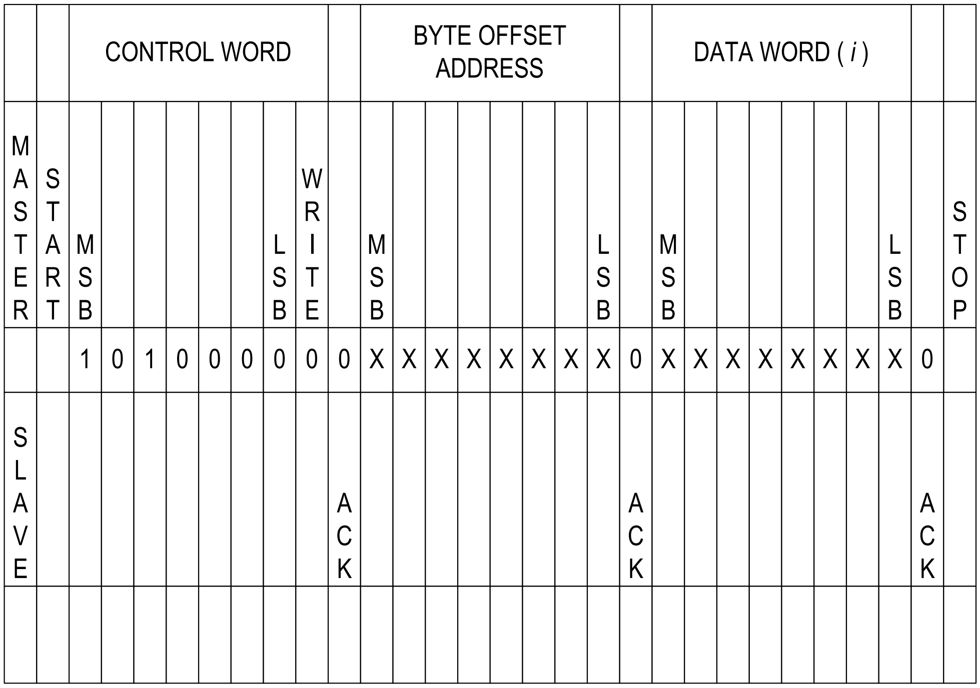

FIGURE 5-1 WRITE BYTE OPERATION

5.3.3 Write Operations (Sequential Write)

The 2-wire slave shall support up to a 4 sequential byte write without repeatedly sending slave address and memory address information. A sequential write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the slave acknowledges receipt of the first data word, the master can transmit up to three more data words. The slave shall send an acknowledge after each data word received. The master must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that 2-wire interface 'combined format' using repeated START conditions is not supported on write commands.

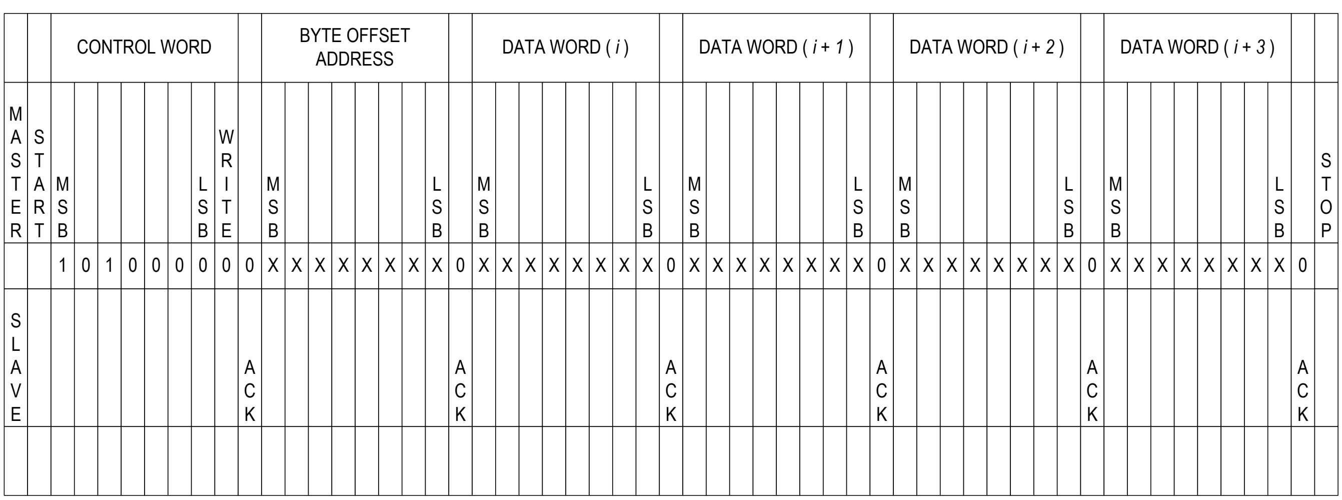

FIGURE 5-2 SEQUENTIAL WRITE OPERATION

5.3.4 Write Operations (Acknowledge Polling)

Once the slave internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the slave respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

5.3.5 Read Operations (Current Address Read)

A current address read operation requires only the slave address read word (10100001) be sent. Once acknowledged by the slave, the current address data word is serially clocked out. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

		CONTROL WORD																		
MASTER	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	
SLAVE										ACK	MSB							LSB		
											DATA WORD (*i*)									

FIGURE 5-3 CURRENT ADDRESS READ

5.3.6 Read Operations (Random Read)

A random read operation requires a dummy write operation to load in the target byte address. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the slave. The master then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The slave acknowledges the device address and serially clocks out the requested data word. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

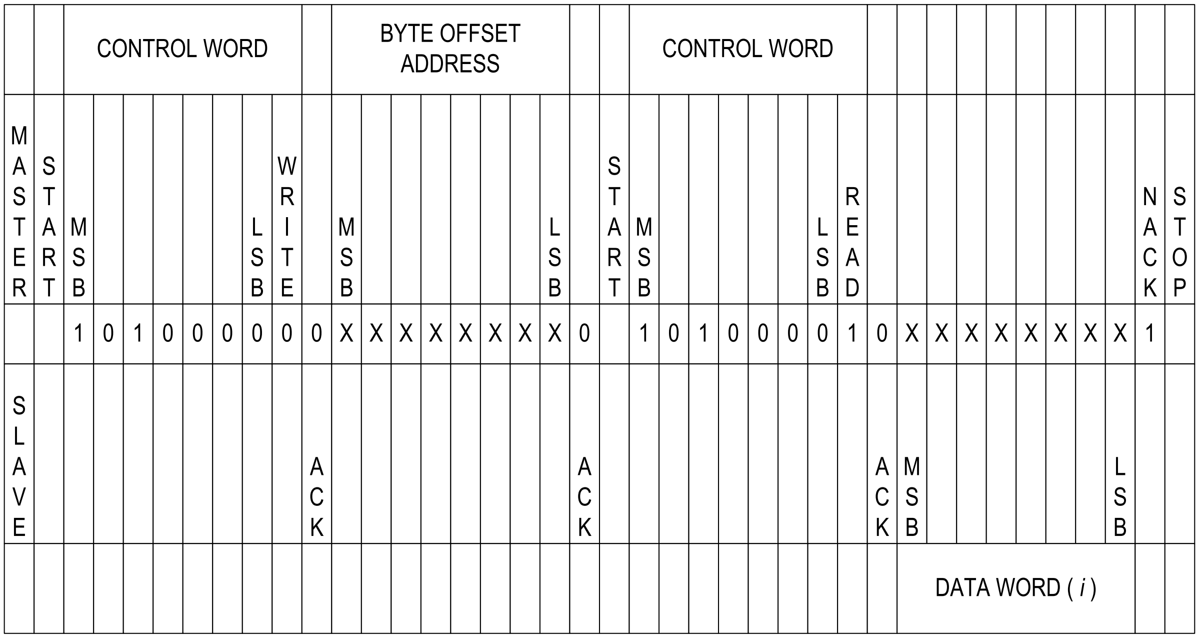

FIGURE 5-4 RANDOM READ

5.3.7 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read or a random address read. To specify a sequential read, the master responds with an acknowledge (instead of a STOP) after each data word. As long as the slave receives an acknowledge, it shall serially clock out sequential data words. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

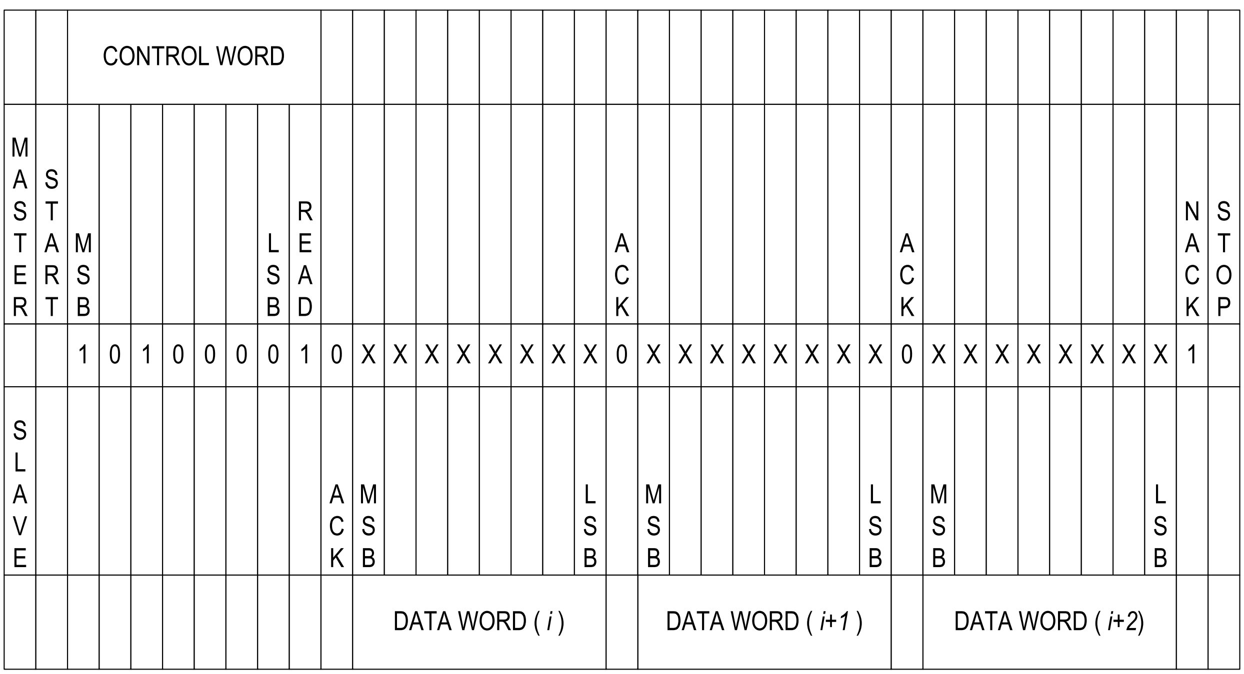

FIGURE 5-5 SEQUENTIAL ADDRESS READ STARTING AT CURRENT ADDRESS

		CONTROL WORD									BYTE OFFSET ADDRESS										CONTROL WORD																																				
MASTER	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1	
SLAVE										ACK									ACK										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
																														DATA WORD (i)									DATA WORD (i+1)									DATA WORD (i+2)									

FIGURE 5-6 SEQUENTIAL ADDRESS READ STARTING WITH RANDOM READ

5.4 2-wire Interface Timing

5.4.1 Timing Diagram

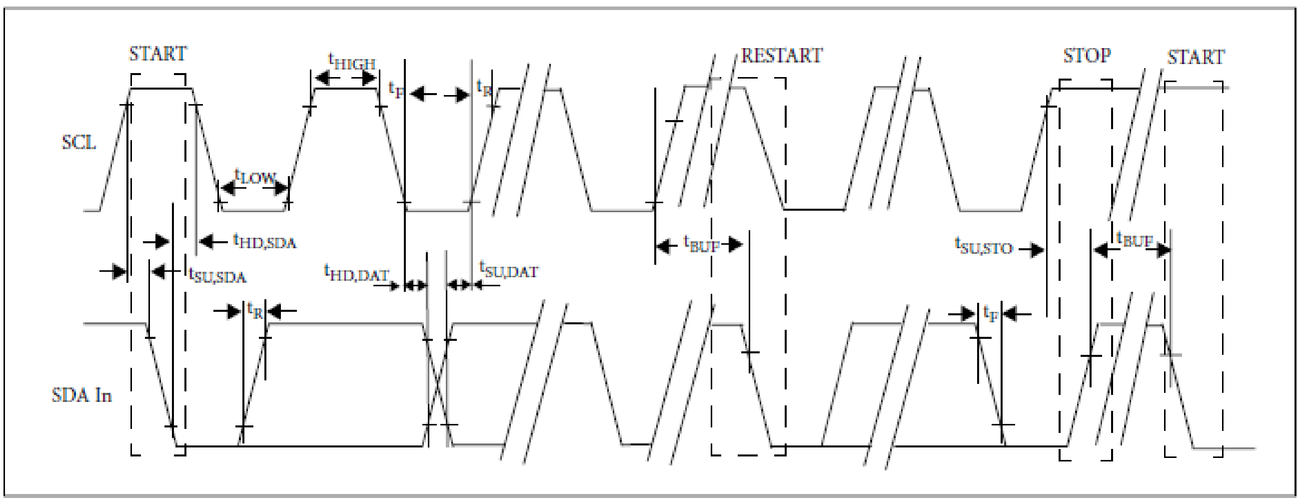

FIGURE 5-7 TIMING DIAGRAM

5.4.2 Timing Parameters

TABLE 5-1 MANAGEMENT INTERFACE TIMING PARAMETERS

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6		us	
Time bus free before new transmission can start	tBUF	20		us	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		us	
START Set-up Time	tSU.STA	0.6		us	
Data In Hold Time	tHD.DAT	0		us	
Data in Set-up Time	tSU.DAT	0.1		us	
Input Rise Time (400 kHz)	tR.400		300	ns	From (VIL,MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400 kHz)	tF.400		300	ns	From (VIH,MIN + 0.15) to (VIL,MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		us	
Serial Interface Clock Holdoff (Clock Stretching)	T_clock_hold		500	us	Maximum time the slave may hold the SCL line low before continuing with a read or write operation

TABLE 5-2 NON-VOLATILE MEMORY SPECIFICATION

Parameter	Symbol	Min	Max	Unit	Conditions
Complete Single or Sequential Write	tWR		40	ms	Complete (up to) 4-byte Write
Endurance (Write Cycles)		50,000		cycles	70C

5.5 Write Operation Restrictions

The 1-byte locations shall be written with single byte write operations, and those >1 byte may be written with multi-byte write operations. The contents of writable memory blocks defined in Table 5-3, except Page 02h, are volatile with all bits set to zero at power on.

TABLE 5-3 WRITABLE MEMORY BLOCKS

Byte	# Bytes	Operation	Description
Page 00h			**Volatile**
86	1	Read/Write	Control Register
87	1	Read/Write	Rx Rate select Register
88	1	Read/Write	Tx Rate select Register
89-92	4	Read/Write	Software Application Select per SFF-8079, Rx channels
93	1	Read/Write	High Power Class Enable / Power Set / Power Override
94-97	4	Read/Write	Software Application Select per SFF-8079, Tx channels
98	1	Read/Write	Tx and Rx CDR Controls
99	1	Read/Write	Reserved
100-104	5	Read/Write	Hardware Interrupt Pin Masking Bits
105-106	2	Read/Write	Vendor Specific
107	1	Read/Write	Reserved
111-112	2	Read/Write	Assigned for use by PCI Express
115-118	4	Read/Write	Reserved
119-122	4	Write-Only	Password Change Entry Area (Optional)
123-126	4	Write-Only	Password Entry Area (Optional)
127	1	Read/Write	Page Select Byte
Page 02h			**Non-Volatile**
128-255	128	Read/Write	User Writable Memory
Page 03h			**Volatile**
226-241	16	Read/Write	Optional Channel Controls
242-251	10	Read/Write	Channel Monitor Masks
252-255	4	Read/Write	Reserved
Page 20h			**Volatile**
140-151	12	Read/Write	Interrupt mask bits for monitored parameters
250	1	Read/Write	Counters reset function

6 Memory Map

6.1 Overview

The memory map is utilized for status, ID, monitoring and control functions.

The map is arranged into a single lower page address space of 128 bytes and multiple upper address pages. This structure permits timely access to addresses in the lower page such as interrupt flags and monitors. Less time critical entries such as serial ID information and threshold settings are available with the page select function. Data used for interrupt handling is located in Lower Page 00h to enable single block read operations for time critical data.

Upper Page 01h and Upper Page 02h are optional. Upper Page 01h allows implementation of application select table while Upper Page 02h provides a user read/write space. Implementation of these two pages is optional. Lower and Upper Page 00h are always implemented. Page 03h is required if Page 00h Byte 2 bit 2 is low.

Upper pages 20h-21h contain support for additional monitored parameters for modules that have PAM4 modulation and/or have optical transmission at 2 wavelengths on a DWDM grid. Page 20h provides the alarms, warnings, masks, parameter values and configuration. Page 21h provides the alarm and warning thresholds. Pages 20h and 21h are required if Page 00 Byte 195 bit 0 is high.

Pages 22-7Fh are reserved for future use. Writing the value of a non-supported page shall not be accepted by the transceiver. The Page Select byte shall revert to 0 and read/write operations shall be to Upper Page 00h. Pages 04-1Fh and 80-FFh are for vendor specific functions.

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	107	Reserved	1	Read/Write
108	110	Free Side Device Properties	3	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	114	Free Side Device Properties	2	Read-Only
115	118	Reserved	4	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write

Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only

Page 01h (Optional)				
128	128	CC_APPS	1	Read-Only
129	129	AST Table Length (TL)	1	Read-Only
130	131	Application Code Entry 0	2	Read-Only
132	133	Application Code Entry 1	2	Read-Only
134	253	Other entries	120	Read-Only
254	255	Application Code Entry TL	2	Read-Only

Page 02h (Optional)				
128	255	User EEPROM Data	128	Read/Write

Page 03h (Optional)				
128	175	Free Side Device Thresholds	48	Read-Only
176	223	Channel Thresholds	48	Read-Only
224	229	Tx EQ, Rx Output and TC Support	6	Read-Only
230	241	Channel Controls	12	Read/Write
242	251	Channel Monitor Masks	10	Read/Write
252	255	Reserved	4	Read/Write

Pages 04h-1Fh (Optional)				
128	255	Vendor Specific	128	Read/Write

Pages 20h-21h (Optional)				
128	255	PAM-4 and WDM Features	128	Read/Write

Pages 22h-7Fh (Optional)				
128	255	Reserved	128	Read/Write

Pages 80h-FFh (Optional)				
128	255	Vendor Specific	128	Read/Write

FIGURE 6-1 COMMON MEMORY MAP

Note: Unless specifically stated otherwise, all informative ID fields must contain accurate data. Using a value of 0 to indicate a field is unspecified (as is common in the SFP definition) is not permitted. Reserved memory locations are to be filled with logic zeros in all bit locations for reserved bytes, and in reserved bit locations for partially specified byte locations.

6.1.1 Required Versus Optional Functionality

The memory map tables contained within this section include columns for passive cables (PC), active cables (AC), active optical cables (AO) and separable modules (SM). Depending on the free side device type, some common memory map parameters are optional. In each column, one of three options is specified: required (R), optional (O) or conditional upon another parameter which is optional (C). Entries with a dash (-) indicate that whether the byte or bit is required is not relevant.

6.2 Lower Page 00h

The 128 bytes of Lower Page 00h are used to access a variety of measurement, diagnostic and control functions. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

TABLE 6-1 LOWER PAGE 00H MEMORY MAP

Byte	Description	Type	PC	AC	AO	SM
0	Identifier (See SFF-8024 Transceiver Management)	Read-Only	R	R	R	R
1-2	Status	Read-Only	See Table 6-2			
3-21	Interrupt Flags	Read-Only	See Table 6-4, Table 6-5 and Table 6-6			
22-33	Free Side Device Monitors	Read-Only	See Table 6-7			
34-81	Channel Monitors	Read-Only	See Table 6-8			
82-85	Reserved	Read-Only	-			
86-98	Control	Read/Write	See Table 6-9			
99	Reserved	Read/Write	-			
100-104	Free Side Device and Channel Masks	Read/Write	See Table 6-14			
105-106	Vendor Specific	Read/Write	-			
107	Reserved	Read/Write	-			
108-110	Free Side Device Properties	Read-Only	See Table 6-15			
111-112	Assigned for use by PCI Express	Read/Write	See Table 6-15			
113-114	Free Side Device Properties	Read-Only	See Table 6-15			
115-118	Reserved	Read/Write	-			
119-122	Password Change Entry Area	Write-Only	O	O	O	O
123-126	Password Entry Area	Write-Only	O	O	O	O
127	Page Select Byte	Read/Write	R	R	R	R

6.2.1 Identifier

Page 00h Byte 0 and Page 00h Byte 128 shall contain the same parameter values. See 6.3.1 for parameter description. See document SFF-8024 Transceiver Management section for definition of valid values.

6.2.2 Status Indicators

TABLE 6-2 STATUS INDICATORS (PAGE 00H BYTES 1-2)

Byte	Bit	Name	Description	PC	AC	AO	SM
1	All	Revision Compliance	See Table 6-3.	R	R	R	R
2	7-4	Reserved	Module State Code – reserved for microQSFP MSA.	-	-	-	-
	3	Reserved		-	-	-	-
	2	Flat_mem	Upper memory flat or paged. Flat memory: 0 = paging, 1 = Page 00h only	R	R	R	R
	1	IntL	Digital state of the IntL Interrupt output pin. 1 = IntL not asserted, 0 = IntL asserted. Default = 1.	R	R	R	R
	0	Data_Not_Ready	Indicates free-side does not yet have valid monitor data. The bit remains high until valid data can be read at which time the bit goes low.	R	R	R	R

The Data_Not_Ready bit shall be asserted high during free-side device reset, power up reset and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down or reset. Upon completion of power up reset, the free-side device shall assert the IntL output signal and bit (if supported) low while de-asserting the Data_Not_Ready bit low. The IntL bit will remain asserted until a read is performed of the Data_Not_Ready bit (Byte 2).

TABLE 6-3 REVISION COMPLIANCE (PAGE 00H BYTE 1)

Value	Memory Map Version
00h	Revision not specified. Do not use for SFF-8636 rev 2.5 or higher.
01h	SFF-8436 Rev 4.8 or earlier
02h	Includes functionality described in revision 4.8 or earlier of SFF-8436, except that this byte and Bytes 186-189 are as defined in this document
03h	SFF-8636 Rev 1.3 or earlier
04h	SFF-8636 Rev 1.4
05h	SFF-8636 Rev 1.5
06h	SFF-8636 Rev 2.0
07h	SFF-8636 Rev 2.5, 2.6 and 2.7
08h	SFF-8636 Rev 2.8 or later
09-FFh	Reserved

6.2.3 Interrupt Flags

Bytes 3-21 consist of interrupt flags for LOS, TX Fault, warnings and alarms. The non-asserted state shall be 0b. If an interrupt flag condition is true, the free side shall assert the corresponding flag bit to 1b. The flag bit shall remain set until the fixed-side performs a read operation of the bit or the free side is reset. Flag bits cleared while underlying interrupt condition remains true may be immediately set again by the free side device. During this process the IntL output signal may be re-asserted if the associated mask bit is not set. These flags may be masked.

TABLE 6-4 CHANNEL STATUS INTERRUPT FLAGS (PAGE 00H BYTES 3-5)

Byte	Bit	Name	Description	PC	AC	AO	SM
3	7	L-Tx4 LOS	Latched TX LOS indicator, channel 4	0	0	0	0
	6	L-Tx3 LOS	Latched TX LOS indicator, channel 3	0	0	0	0
	5	L-Tx2 LOS	Latched TX LOS indicator, channel 2	0	0	0	0
	4	L-Tx1 LOS	Latched TX LOS indicator, channel 1	0	0	0	0
	3	L-Rx4 LOS	Latched RX LOS indicator, channel 4	0	0	0	0
	2	L-Rx3 LOS	Latched RX LOS indicator, channel 3	0	0	0	0
	1	L-Rx2 LOS	Latched RX LOS indicator, channel 2	0	0	0	0
	0	L-Rx1 LOS	Latched RX LOS indicator, channel 1	0	0	0	0
4	7	L-Tx4 Adapt EQ Fault	Latched TX input Adaptive EQ fault indicator, channel 4 (if supported)	0	0	0	0
	6	L-Tx3 Adapt EQ Fault	Latched TX input Adaptive EQ fault indicator, channel 3 (if supported)	0	0	0	0
	5	L-Tx2 Adapt EQ Fault	Latched TX input Adaptive EQ fault indicator, channel 2 (if supported)	0	0	0	0
	4	L-Tx1 Adapt EQ Fault	Latched TX input Adaptive EQ fault indicator, channel 1 (if supported)	0	0	0	0
	3	L-Tx4 Fault	Latched TX Transmitter/Laser fault indicator, channel 4	0	0	0	R
	2	L-Tx3 Fault	Latched TX Transmitter/Laser fault indicator, channel 3	0	0	0	R
	1	L-Tx2 Fault	Latched TX Transmitter/Laser fault indicator, channel 2	0	0	0	R
	0	L-Tx1 Fault	Latched TX Transmitter/Laser fault indicator, channel 1	0	0	0	R
5	7	L-Tx4 LOL	Latched TX CDR LOL indicator, ch 4	0	0	0	0
	6	L-Tx3 LOL	Latched TX CDR LOL indicator, ch 3	0	0	0	0
	5	L-Tx2 LOL	Latched TX CDR LOL indicator, ch 2	0	0	0	0
	4	L-Tx1 LOL	Latched TX CDR LOL indicator, ch 1	0	0	0	0
	3	L-Rx4 LOL	Latched RX CDR LOL indicator, ch 4	0	0	0	0
	2	L-Rx3 LOL	Latched RX CDR LOL indicator, ch 3	0	0	0	0
	1	L-Rx2 LOL	Latched RX CDR LOL indicator, ch 2	0	0	0	0
	0	L-Rx1 LOL	Latched RX CDR LOL indicator, ch 1	0	0	0	0

TABLE 6-5 FREE SIDE MONITOR INTERRUPT FLAGS (PAGE 00H BYTES 6-8)

Byte	Bit	Name	Description	PC	AC	AO	SM
6	7	L-Temp High Alarm	Latched high temperature alarm	0	0	0	R
	6	L-Temp Low Alarm	Latched low temperature alarm	0	0	0	0
	5	L-Temp High Warning	Latched high temperature warning	0	0	0	0
	4	L-Temp Low Warning	Latched low temperature warning	0	0	0	0
	3-2	Reserved		-	-	-	-
	1	TC readiness flag	Asserted (one) after TC has stabilized. Returns to zero when read. Does not reassert until the module is reset or re-enters high power mode from low power mode. See Table 6-26 for the TC Readiness Implemented bit.	0	0	0	0
	0	Initialization complete flag	Asserted (one) after initialization and/or reset has completed. Returns to zero when read. Does not reassert unless reset. See Table 6-26 for the Initialization Complete Implemented bit.	0	0	0	0
7	7	L-Vcc High Alarm	Latched high supply voltage alarm	0	0	0	0
	6	L-Vcc Low Alarm	Latched low supply voltage alarm	0	0	0	0
	5	L-Vcc High Warning	Latched high supply voltage warning	0	0	0	0
	4	L-Vcc Low Warning	Latched low supply voltage warning	0	0	0	0
	3-0	Reserved		-	-	-	-
8	All	Vendor Specific		-	-	-	-

TABLE 6-6 CHANNEL MONITOR INTERRUPT FLAGS (PAGE 00H BYTES 9-21)

Byte	Bit	Name	Description	PC	AC	AO	SM
9	7	L-Rx1 Power High Alarm	Latched high RX power alarm, channel 1	0	0	0	0
	6	L-Rx1 Power Low Alarm	Latched low RX power alarm, channel 1	0	0	0	0
	5	L-Rx1 Power High Warning	Latched high RX power warning, channel 1	0	0	0	0
	4	L-Rx1 Power Low Warning	Latched low RX power warning, channel 1	0	0	0	0
	3	L-Rx2 Power High Alarm	Latched high RX power alarm, channel 2	0	0	0	0
	2	L-Rx2 Power Low Alarm	Latched low RX power alarm, channel 2	0	0	0	0
	1	L-Rx2 Power High Warning	Latched high RX power warning, channel 2	0	0	0	0
	0	L-Rx2 Power Low Warning	Latched low RX power warning, channel 2	0	0	0	0
10	7	L-Rx3 Power High Alarm	Latched high RX power alarm, channel 3	0	0	0	0
	6	L-Rx3 Power Low Alarm	Latched low RX power alarm, channel 3	0	0	0	0
	5	L-Rx3 Power High Warning	Latched high RX power warning, channel 3	0	0	0	0
	4	L-Rx3 Power Low Warning	Latched low RX power warning, channel 3	0	0	0	0
	3	L-Rx4 Power High Alarm	Latched high RX power alarm, channel 4	0	0	0	0
	2	L-Rx4 Power low Alarm	Latched low RX power alarm, channel 4	0	0	0	0
	1	L-Rx4 Power high Warning	Latched high RX power warning, channel 4	0	0	0	0
	0	L-Rx4 Power low warning	Latched low RX power warning, channel 4	0	0	0	0
11	7	L-Tx1 Bias High Alarm	Latched high TX bias alarm, channel 1	0	0	0	0
	6	L-Tx1 Bias Low Alarm	Latched low TX bias alarm, channel 1	0	0	0	0
	5	L-Tx1 Bias high Warning	Latched high TX bias warning, channel 1	0	0	0	0
	4	L-Tx1 Bias Low Warning	Latched low TX bias warning, channel 1	0	0	0	0
	3	L-Tx2 Bias High Alarm	Latched high TX bias alarm, channel 2	0	0	0	0
	2	L-Tx2 Bias Low Alarm	Latched low TX bias alarm, channel 2	0	0	0	0
	1	L-Tx2 Bias High Warning	Latched High TX bias warning, channel 2	0	0	0	0
	0	L-Tx2 Bias Low Warning	Latched low TX bias warning, channel 2	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
12	7	L-Tx3 Bias High Alarm	Latched high TX bias alarm, channel 3	0	0	0	0
	6	L-Tx3 Bias Low Alarm	Latched low TX bias alarm, channel 3	0	0	0	0
	5	L-Tx3 Bias High Warning	Latched high TX bias warning, channel 3	0	0	0	0
	4	L-Tx3 Bias Low Warning	Latched low TX bias warning, channel 3	0	0	0	0
	3	L-Tx4 Bias High Alarm	Latched high TX bias alarm, channel 4	0	0	0	0
	2	L-Tx4 Bias Low Alarm	Latched low TX bias alarm, Channel 4	0	0	0	0
	1	L-Tx4 Bias High Warning	Latched high TX bias warning, channel 4	0	0	0	0
	0	L-Tx4 Bias Low Warning	Latched low TX bias warning, channel 4	0	0	0	0
13	7	L-Tx1 Power High Alarm	Latched high TX Power alarm, channel 1	0	0	0	0
	6	L-Tx1 Power Low Alarm	Latched low TX Power alarm, channel 1	0	0	0	0
	5	L-Tx1 Power High Warning	Latched high TX Power warning, channel 1	0	0	0	0
	4	L-Tx1 Power Low Warning	Latched low TX Power warning, channel 1	0	0	0	0
	3	L-Tx2 Power High Alarm	Latched high TX Power alarm, channel 2	0	0	0	0
	2	L-Tx2 Power Low Alarm	Latched low TX Power alarm, channel 2	0	0	0	0
	1	L-Tx2 Power High Warning	Latched High TX Power warning, channel 2	0	0	0	0
	0	L-Tx2 Power Low Warning	Latched low TX Power warning, channel 2	0	0	0	0
14	7	L-Tx3 Power High Alarm	Latched high TX Power alarm, channel 3	0	0	0	0
	6	L-Tx3 Power Low Alarm	Latched low TX Power alarm, channel 3	0	0	0	0
	5	L-Tx3 Power High Warning	Latched high TX Power warning, channel 3	0	0	0	0
	4	L-Tx3 Power Low Warning	Latched low TX Power warning, channel 3	0	0	0	0
	3	L-Tx4 Power High Alarm	Latched high TX Power alarm, channel 4	0	0	0	0
	2	L-Tx4 Power Low Alarm	Latched low TX Power alarm, Channel 4	0	0	0	0
	1	L-Tx4 Power High Warning	Latched high TX Power warning, channel 4	0	0	0	0
	0	L-Tx4 Power Low Warning	Latched low TX Power warning, channel 4	0	0	0	0
15-16	All	Reserved	Reserved channel monitor flags, set 4	-	-	-	-
17-18	All	Reserved	Reserved channel monitor flags, set 5	-	-	-	-
19-20	All	Vendor Specific		-	-	-	-
21	All	Vendor Specific		-	-	-	-

6.2.4 Free Side Device Monitors

Real time monitoring for the free side device includes temperature, supply voltage, and monitoring for each transmit and receive channel.

The fixed side shall use single 2-byte reads to retrieve all 16-bit data to guarantee data coherency. The free side device shall prevent the host from acquiring partially updated multi-byte data during a 2-byte read. Clock stretching provides one mechanism to delay the delivery of data until all bytes of one field have been updated. The data format may facilitate greater resolution and range than required. Reference of the specific product specification of the free side device or interoperability standard is necessary to determine the measurement accuracy.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

TABLE 6-7 FREE SIDE MONITORING VALUES (PAGE 00H BYTES 22-33)

Byte	Bit	Name	Description	PC	AC	AO	SM
22	All	Temperature MSB	Internally measured temperature (MSB)	O	O	O	R
23	All	Temperature LSB	Internally measured temperature (LSB)	O	O	O	R
24-25	All	Reserved		-	-	-	-
26	All	Supply Voltage MSB	Internally measured supply voltage (MSB)	O	O	O	O
27	All	Supply Voltage LSB	Internally measured supply voltage (LSB)	O	O	O	O
28-29	All	Reserved		-	-	-	-
30-33	All	Vendor Specific		-	-	-	-

Internally measured free side device temperatures are represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128C to +128C that is considered valid between -40C and +125C. Temperature accuracy is Vendor Specific but must be better than +/-3C over specified operating temperature and voltage. Placement of the temperature sensor is vendor specific.

Internally measured free side device supply voltages are represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 to 65535) with LSB equal to 100 uV, yielding a total measurement range of 0 to +6.55 V. Practical considerations to be defined by free side device manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is Vendor Specific but must be better than +/-3% of the manufacturer's nominal value over specified operating temperature and voltage.

6.2.5 Channel Monitors

Real time channel monitoring for each transmit and receive channel includes optical input power and TX bias current.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

TABLE 6-8 CHANNEL MONITORING VALUES (PAGE 00H BYTES 34-81)

Byte	Bit	Name	Description	PC	AC	AO	SM
34	All	Rx1 Power MSB	Internally measured RX input power, channel 1	0	0	0	0
35	All	Rx1 Power LSB		0	0	0	0
36	All	Rx2 Power MSB	Internally measured RX input power, channel 2	0	0	0	0
37	All	Rx2 Power LSB		0	0	0	0
38	All	Rx3 Power MSB	Internally measured RX input power, channel 3	0	0	0	0
39	All	Rx3 Power LSB		0	0	0	0
40	All	Rx4 Power MSB	Internally measured RX input power, channel 4	0	0	0	0
41	All	Rx4 Power LSB		0	0	0	0
42	All	Tx1 Bias MSB	Internally measured TX bias, channel 1	0	0	0	0
43	All	Tx1 Bias LSB		0	0	0	0
44	All	Tx2 Bias MSB	Internally measured TX bias, channel 2	0	0	0	0
45	All	Tx2 Bias LSB		0	0	0	0
46	All	Tx3 Bias MSB	Internally measured TX bias, channel 3	0	0	0	0
47	All	Tx3 Bias LSB		0	0	0	0
48	All	Tx4 Bias MSB	Internally measured TX bias, channel 4	0	0	0	0
49	All	Tx4 Bias LSB		0	0	0	0
50	All	Tx1 Power MSB	Internally measured TX Power, channel 1	0	0	0	0
51	All	Tx1 Power LSB		0	0	0	0
52	All	Tx2 Power MSB	Internally measured TX Power, channel 2	0	0	0	0
53	All	Tx2 Power LSB		0	0	0	0
54	All	Tx3 Power MSB	Internally measured TX Power, channel 3	0	0	0	0
55	All	Tx3 Power LSB		0	0	0	0
56	All	Tx4 Power MSB	Internally measured TX Power, channel 4	0	0	0	0
57	All	Tx4 Power LSB		0	0	0	0
58-65		Reserved channel monitor set 4		-	-	-	-
66-73		Reserved channel monitor set 5		-	-	-	-
74-81		Vendor Specific		-	-	-	-

Measured TX bias current is represented in mA as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 2 uA, yielding a total measurement range of 0 to 131 mA. Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured RX received optical power is represented in mW as either an average received power or OMA depending upon how Page 00h Byte 220 bit 3 is set. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is Vendor Specific.

Measured TX optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage.

6.2.6 Control Functions

TABLE 6-9 CONTROL FUNCTION BYTES (PAGE 00H BYTES 86-99)

Byte	Bit	Name	Description	PC	AC	AO	SM
86	7-4	Reserved		-	-	-	-
	3	Tx4 Disable	Read/Write bit that allows software disable of transmitters *	-	O	O	R
	2	Tx3 Disable	Read/Write bit that allows software disable of transmitters *	-	O	O	R
	1	Tx2 Disable	Read/Write bit that allows software disable of transmitters *	-	O	O	R
	0	Tx1 Disable	Read/Write bit that allows software disable of transmitters *	-	O	O	R
	* For the case of an electrical/optical transceiver, writing '1' disables the laser of the channel						
87	7	Rx4_Rate_select	Software rate select. Rx Channel 4 MSB	-	O	O	O
	6	Rx4_Rate_select	Software rate select. Rx Channel 4 LSB	-	O	O	O
	5	Rx3_Rate_select	Software rate select. Rx Channel 3 MSB	-	O	O	O
	4	Rx3_Rate_select	Software rate select. Rx Channel 3 LSB	-	O	O	O
	3	Rx2_Rate_select	Software rate select. Rx Channel 2 MSB	-	O	O	O
	2	Rx2_Rate_select	Software rate select. Rx Channel 2 LSB	-	O	O	O
	1	Rx1_Rate_select	Software rate select. Rx Channel 1 MSB	-	O	O	O
	0	Rx1_Rate_select	Software rate select. Rx Channel 1 LSB	-	O	O	O
88	7	Tx4_Rate_select	Software rate select. Tx Channel 4 MSB	-	O	O	O
	6	Tx4_Rate_select	Software rate select. Tx Channel 4 LSB	-	O	O	O
	5	Tx3_Rate_select	Software rate select. Tx Channel 3 MSB	-	O	O	O
	4	Tx3_Rate_select	Software rate select. Tx Channel 3 LSB	-	O	O	O
	3	Tx2_Rate_select	Software rate select. Tx Channel 2 MSB	-	O	O	O
	2	Tx2_Rate_select	Software rate select. Tx Channel 2 LSB	-	O	O	O
	1	Tx1_Rate_select	Software rate select. Tx Channel 1 MSB	-	O	O	O
	0	Tx1_Rate_select	Software rate select. Tx Channel 1 LSB	-	O	O	O
89	All	Rx4_Application_Select	Software Application Select per SFF-8079, Rx Channel 4	-	O	O	O
90	All	Rx3_Application_Select	Software Application Select per SFF-8079, Rx Channel 3	-	O	O	O
91	All	Rx2_Application_Select	Software Application Select per SFF-8079, Rx Channel 2	-	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
92	All	Rx1_Application_Select	Software Application Select per SFF-8079, Rx Channel 1	-	O	O	O
93	7-3	Reserved		-	-	-	-
	2	High Power Class Enable (Classes 5-7)	1b = allow Power Classes 1-7 in High Power Mode. 0b = allow Power Classes 1-4 in High Power Mode. See 6.3.2 for details of power classes. Default 0.	-	O	O	O
	1	Power set	For QSFP+/QSFP28: 1b = Set to Low Power Mode. 0b = Set to High Power Mode. Bit is ignored if Power override = 0. Default 0. For microQSFP: Redefined as Low Power Mode. Default=1.	-	R	R	R
	0	Power override	1b = LPMode signal replaced by Power set bit. 0b = LPMode signal controls Power Mode. Default 0.	-	R	R	R
94	All	Tx4_Application_Select	Software application per SFF-8079, Tx Channel 4	-	O	O	O
95	All	Tx3_Application_Select	Software application per SFF-8079, Tx Channel 3	-	O	O	O
96	All	Tx2_Application_Select	Software application per SFF-8079, Tx Channel 2	-	O	O	O
97	All	Tx1_Application_Select	Software application per SFF-8079, Tx Channel 1	-	O	O	O
98	7	Tx4_CDR_control	Channel 4 TX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	6	Tx3_CDR_control	Channel 3 TX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	5	Tx2_CDR_control	Channel 2 TX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	4	Tx1_CDR_control	Channel 1 TX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	3	Rx4_CDR_control	Channel 4 RX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	2	Rx3_CDR_control	Channel 3 RX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	1	Rx2_CDR_control	Channel 2 RX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	0	Rx1_CDR_control	Channel 1 RX CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
99	All	Reserved		-	-	-	-

For transceivers with CDR capability, setting the CDR to ON engages the internal retiming function. Setting the CDR to OFF enables an internal bypassing mode, which directs traffic around the internal CDR. The two most common reasons to turn a CDR off (i.e. internally bypass it) are to run at bit rates not supported by a particular CDR or to save the thermal power in applications where CDR jitter mitigation is not required. Jitter specifications of the high speed interfaces are outside the scope of this specification.

QSFP+ and QSFP28 modules have the LPMode input signal (see SFF-8679) that can be used by the host system to force the module into Low Power Mode. Low Power Mode for those modules is defined as a maximum power consumption of 1.5W. If the LPMode input signal is pulled low by the host system, the module is then capable of entering High Power Mode. The maximum power consumption in High Power Mode depends on the module Power Class as advertised in the Extended Identifier (see 6.3.2), Page 00h, byte 129, bits 1-0 and 7-6.

The operation of the LPMode input signal can be overridden by the host writing a ‘1’ to byte 93, bit 0. In that case, the function of the LPMode input signal is replaced by byte 93, bit 1.

SFF-8436 has 4 power classes from 1.5 to 3.5 W. Only bits 7-6 are used to define those power classes. At revision 1.9 of this specification, 3 new higher power classes, 4.0 W, 4.5 W and 5.0 W were added. These power classes, designated power classes 5, 6 and 7, are designated using bits 1-0 of the Extended Identifier byte, page 00h byte 129. In order to protect legacy host systems designed to support only the original 4 power classes, the High Power Class Enable control was defined at byte 93, bit 2. Modules in power classes 5, 6 or 7 are required to limit power consumption to no more than a power class 4 module if the High Power Class Enable control is not set. They are not required to be functional in this situation.

A truth table for the power controls in byte 93 bits 0, 1 and 2, is shown in Table 6-10.

Power class limits and controls for microQSFP modules are different from the description here. Refer to the MSA specification for details.

TABLE 6-10 TRUTH TABLE FOR ENABLING POWER CLASSES (PAGE 00H BYTE 93)

(The maximum consumption limits in this table are based on SFF-8679 for QSFP modules).

Module Power Class	Ext. Identifier P00h Byte 129				Controls Byte 93			LPMode Input Signal	Maximum Consumption (W)
	[1]	[0]	[7]	[6]	[0]	[1]	[2]		
1 (1.5W)	0	0	0	0	X	X	X	X	1.5
2 (2.0W)	0	0	0	1	0	X	X	High	1.5*
					0	X	X	Low	2.0
					1	1	X	X	1.5*
					1	0	X	X	2.0
3 (2.5W)	0	0	1	0	0	X	X	High	1.5*
					0	X	X	Low	2.5
					1	1	X	X	1.5*
					1	0	X	X	2.5
4 (3.5W)	0	0	1	1	0	X	X	High	1.5*
					0	X	X	Low	3.5
					1	1	X	X	1.5*
					1	0	X	X	3.5
5 (4.0W)	0	1	1	1	0	X	X	High	1.5*
					0	X	0	Low	3.5**
					0	X	1	Low	4.0
					1	1	X	X	1.5*
					1	0	0	X	3.5**
					1	0	1	X	4.0
6 (4.5W)	1	0	1	1	0	X	X	High	1.5*
					0	X	0	Low	3.5**
					0	X	1	Low	4.5
					1	1	X	X	1.5*
					1	0	0	X	3.5**
					1	0	1	X	4.5
7 (5.0W)	1	1	1	1	0	X	X	High	1.5*
					0	X	0	Low	3.5**
					0	X	1	Low	5.0
					1	1	X	X	1.5*
					1	0	0	X	3.5**
					1	0	1	X	5.0

*= Module is held in Low-Power Mode and is not required to be fully functional
** = Module is limited to the dissipation of power class 4 and is not required to be fully functional.

6.2.7 Rate Select

Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple bit rates. In addition, rate selection allows the transmitter to be fine-tuned for specific bit rate transmissions.

The free side device shall implement one of the three options:

a) Provide no support for rate selection
b) Rate selection using extended rate select
c) Rate selection with application select tables

6.2.7.1 No Rate Selection Support

When no rate selection is supported, (Page 00h Byte 221 bits 2 and 3) have a value of 0 and Options (Page 00h Byte 195 bit 5) has a value of 0. Lack of implementation does not indicate lack of simultaneous compliance with multiple standard rates. See 6.3.4 for the description of how compliance with particular standards should be determined.

6.2.7.2 Extended Rate Selection

When Page 00h Byte 195 bit 5 is 1 and Rate Select declaration bits (Page 00h Byte 221 bits 2 and 3) have the values of 0 and 1 respectively and at least one of the bits in the Extended Rate Compliance byte (Page 00h Byte 141) has a value of one, the free side device supports extended rate select. For extended rate selection, two bits are assigned to each receiver in Byte 87 (Rxn_Rate_Select) and two bits for each transmitter in Byte 88 (Txn_Rate_Select) to specify up to four bit rates. See Table 6-11 for the functionality when Byte 141 bits 0-1 are set. All other values of the Extended Rate Compliance byte are reserved.

TABLE 6-11 XN_RATE_SELECT WITH EXTENDED RATE SELECTION

xN_Rate_Select (MSB Value)	xN_Rate_Select (LSB Value)	Description
Version 1 - Page 00h Byte 141 Bit 0 = 1		
0	0	Optimized for bit rates less than 2.2 Gbps
0	1	Optimized for bit rates from 2.2 up to 6.6 Gbps
1	0	Optimized for 6.6 Gbps bit rates and above
1	1	Reserved
Version 2 - Page 00h Byte 141 Bit 1 = 1		
0	0	Optimized for bit rates less than 12 Gbps
0	1	Optimized for bit rates from 12 up to 24 Gbps
1	0	Optimized for bit rates from 24 up to 26 Gbps
1	1	Optimized for 26 Gbps bit rates and above

6.2.7.3 Rate Selection Using Application Select Tables

When the Rate Select declaration bits (Page 00h Byte 221 bits 2-3) have the values of 1 and 0 respectively, the Application Select method defined in Page 01h is used (see 6.4, SFF-8079 and SFF-8089). The fixed side reads the entire application select table on Page 01h to determine the capabilities of the free side. The fixed side controls each channel separately by writing a Control Mode and Table Select (TS) byte to Bytes 89-92 and Bytes 94-97.

TABLE 6-12 APPLICATION SELECT (PAGE 00H BYTES 89-92 AND BYTES 94-97)

7	6	5	4	3	2	1	0
Control Mode		Table Select TS					

Control Mode defines the application control mode. Table Select selects the free side device behavior from the Application Select Table (page 01h) among 63 possibilities (000000 to 111110). Note that (111111) is invalid.

TABLE 6-13 CONTROL MODE DEFINITION

Bit 7	Bit 6	Function	Bytes 87-88 Control	Table Select Control
0	0	Extended rate selection	LSB and MSB are used according to declaration bits.	Ignored
1	Don't care	Application select	Ignored	field points to application

Note: Default values for control mode is 00 and is volatile memory.

6.2.8 Free Side Device Indicators and Channel Masks

The fixed side may control which flags result in a hardware interrupt by setting high individual bits from a set of masking bits in Page 00h Bytes 100-104 for free side device flags, and Page 03h Bytes 242-251 for channel flags. See Table 6-14 and Table 6-37. A 1 value in a masking bit prevents the assertion of the hardware interrupt pin, if one exists, by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0).

The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually reassert the hardware interrupt pin. A mask bit is allocated for each flag bit.

TABLE 6-14 HARDWARE INTERRUPT PIN MASKING BITS (PAGE 00H BYTES 100-106)

Byte	Bit	Name	Description	PC	AC	AO	SM
100	7	M-Tx4 LOS Mask	Masking Bit for TX LOS indicator, channel 4	C	C	C	C
	6	M-Tx3 LOS Mask	Masking Bit for TX LOS indicator, channel 3	C	C	C	C
	5	M-Tx2 LOS Mask	Masking Bit for TX LOS indicator, channel 2	C	C	C	C
	4	M-Tx1 LOS Mask	Masking Bit for TX LOS indicator, channel 1	C	C	C	C
	3	M-Rx4 LOS Mask	Masking Bit for RX LOS indicator, channel 4	C	C	C	C
	2	M-Rx3 LOS Mask	Masking Bit for RX LOS indicator, channel 3	C	C	C	C
	1	M-Rx2 LOS Mask	Masking Bit for RX LOS indicator, channel 2	C	C	C	C
	0	M-Rx1 LOS Mask	Masking Bit for RX LOS indicator, channel 1	C	C	C	C
101	7	M-Tx4 Adapt EQ Fault Mask	Masking Bit for TX, Adaptive EQ fault indicator, channel 4	C	C	C	C
	6	M-Tx3 Adapt EQ Fault Mask	Masking Bit for TX, Adaptive EQ fault indicator, channel 3	C	C	C	C
	5	M-Tx2 Adapt EQ Fault Mask	Masking Bit for TX, Adaptive EQ fault indicator, channel 2	C	C	C	C
	4	M-Tx1 Adapt EQ Fault Mask	Masking Bit for TX, Adaptive EQ fault indicator, channel 1	C	C	C	C
	3	M-Tx4 Transmitter Fault Mask	Masking Bit for TX Transmitter/Laser indicator, channel 4	C	C	C	R
	2	M-Tx3 Transmitter Fault Mask	Masking Bit for TX Transmitter/Laser indicator, channel 3	C	C	C	R
	1	M-Tx2 Transmitter Fault Mask	Masking Bit for TX Transmitter/Laser indicator, channel 2	C	C	C	R

Byte	Bit	Name	Description	PC	AC	AO	SM
	0	M-Tx1 Transmitter Fault Mask	Masking Bit for TX Transmitter/Laser indicator, channel 1	C	C	C	R
102	7	M-Tx4 CDR LOL Mask	Masking Bit for TX CDR Loss of Lock indicator, channel 4	C	C	C	C
	6	M-Tx3 CDR LOL Mask	Masking Bit for TX CDR Loss of Lock indicator, channel 3	C	C	C	C
	5	M-Tx2 CDR LOL Mask	Masking Bit for TX CDR Loss of Lock indicator, channel 2	C	C	C	C
	4	M-Tx1 CDR LOL Mask	Masking Bit for TX CDR Loss of Lock indicator, channel 1	C	C	C	C
	3	M-Rx4 CDR LOL Mask	Masking Bit for RX CDR Loss of Lock indicator, channel 4	C	C	C	C
	2	M-Rx3 CDR LOL Mask	Masking Bit for RX CDR Loss of Lock indicator, channel 3	C	C	C	C
	1	M-Rx2 CDR LOL Mask	Masking Bit for RX CDR Loss of Lock indicator, channel 2	C	C	C	C
	0	M-Rx1 CDR LOL Mask	Masking Bit for RX CDR Loss of Lock indicator, channel 1	C	C	C	C
103	7	M-Temp High Alarm	Masking Bit for high Temperature alarm	C	C	C	C
	6	M-Temp Low Alarm	Masking Bit for low Temperature alarm	C	C	C	C
	5	M- Temp High Warning	Masking Bit for high Temperature warning	C	C	C	C
	4	M-Temp Low Warning	Masking Bit for low Temperature warning	C	C	C	C
	3-2	Reserved		-	-	-	-
	1	M-TC readiness flag	Masking Bit for TC readiness flag	C	C	C	C
	0	Reserved		-	-	-	-
104	7	M-Vcc High alarm	Masking Bit for high Vcc alarm	C	C	C	C
	6	M-Vcc Low alarm	Masking Bit for low Vcc alarm	C	C	C	C
	5	M-Vcc High Warning	Masking Bit for high Vcc warning	C	C	C	C
	4	M-Vcc Low Warning	Masking Bit for low Vcc warning	C	C	C	C
	3-0	Reserved		-	-	-	-
105-106	All	Vendor Specific		-	-	-	-

6.2.9 Free Side Device Properties

The unsigned 16-bit value in Bytes 108-109 indicates the propagation delay of the non-separable free side device. Byte 108 bit 7 is the most significant bit and Byte 109 bit 0 is the least significant. Each unit of the combined value corresponds to 10 ns with fractional values rounded up to the next unit.

Byte 110 bits 7-4 specify the free-side device power consumption levels below 1.5 W. A value of 0000 shall indicate that a power consumption limit below 1.5 W is not available. A value of 0001 shall indicates the free-side device shall consume no more than 1 W, 0010 indicates no more than 0.75 W and 0011 indicates no more than 0.5 W.

A value of 1 in Byte 110 bit 3 shall indicate that both ends of the free-side device comply with the SFF-8636 specification. A value of 0 shall be utilized for all other cases including use of other management interfaces specifications and separable applications where the free-side device ends and media can be physically separated from each other. Byte 110 bits 2-0 indicate that the free-side device can operate properly from less than nominal 3.3 V on the Vcc pins. A value of 000 indicates the feature is disabled. The free-side device shall operate properly from nominal 2.5 V with a value of 001 and nominal 1.8 V with a value of 010.

The use of Bytes 111-112 is not defined in this specification.

Byte 113 bits 3-0 specify which channels of the free side device at the near end are implemented. A value of 0 indicates that the channel is implemented and a value of 1 indicates that the channel is not implemented.

Byte 113 bits 6-4 are used to indicate what type of device(s) are implemented at the far end(s) of a cable or module. A separable free side device or a device that does not specify the far end implementation is coded 000.

TABLE 6-15 FREE SIDE DEVICE PROPERTIES (PAGE 00H BYTES 108-114)

Byte	Bit	Name	Description	PC	AC	AO	SM
108	All	Propagation Delay MSB	Most significant byte of propagation delay	R	R	R	O
109	All	Propagation Delay LSB	Least significant byte of propagation delay	R	R	R	O
110	7-4	Advanced Low Power Mode	Code indicates maximum power consumption less than 1.5 W. 0000 1.5W or higher 0001 no more than 1 W 0010 no more than 0.75 W 0011 no more than 0.5 W	R	R	R	O
	3	Far Side Managed	A value of 1 indicates that the far end is managed and complies with SFF-8636.	R	R	R	O
	2-0	Min Operating Voltage	Code indicates nominal supply voltages lower than 3.3 V. 000 3.3 V 001 2.5 V 010 1.8 V	R	R	R	O
111-112	All	Assigned for use by PCI Express	Used for: - The PCI Express External Cable Specification - The PCI Express OCuLink Specification	-	-	-	-
113	7	Reserved		-	-	-	-
	6-4	Far End Implementation	=000 Far end is unspecified =001 Cable with single far end with 4 channels implemented, or separable module with 4-channel connector =010 Cable with single far end with 2 channels implemented, or separable module with 2-channel connector =011 Cable with single far end with 1 channel implemented, or separable module with 1-channel connector =100 4 far ends with 1 channel implemented in each (i.e. 4x1 break out) =101 2 far ends with 2 channels implemented in each (i.e. 2x2 break out) =110 2 far ends with 1 channel implemented in each (i.e. 2x1 break out)	R	R	R	O
	3-0	Near End Implementation	Bit 0 =0 Channel 1 implemented =1 Channel 1 not implemented Bit 1 =0 Channel 2 implemented =1 Channel 2 not implemented Bit 2 =0 Channel 3 implemented =1 Channel 3 not implemented Bit 3 =0 Channel 4 implemented =1 Channel 4 not implemented	R	R	R	O
114	7-4	Tx_TurnOn MaxDuration	Tx_TurnOn_MaxDuration for microQSFP MSA. 0000b=Not implemented.	R	R	R	R
	3-0	DatapathInit MaxDuration	DataPathInit_MaxDuration for microQSFP MSA. 0000b=Not implemented.	R	R	R	R

6.2.10 Password Entry and Change

Bytes 119-126 are reserved for an optional password entry function. The Password entry bytes are write only and will be retained until power down, reset, or rewritten by fixed side. This function may be used to control read/write access to Vendor Specific Page 02h. Additionally, free side device vendors may use this function to implement write protection of Serial ID and other read only information. Passwords may be supplied to and used by fixed side system manufacturers to limit write access in the User EEPROM Page 02h.

Password access shall not be required to access free side device data in the lower memory Page 00h or in Upper Page 00h, 02h and 03h. Note that multiple manufacturer passwords may be defined to allow selective access to read or write to various sections of memory as allowed above.

Fixed side manufacturer and free side device manufacturer passwords shall be distinguished by the high order bit (bit 7, Byte 123). All fixed side manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all free side device manufacturer passwords in the range of 80000000h to FFFFFFFFh. Fixed side system manufacturer passwords shall be initially set to 00001011h in new free side devices.

Fixed side system manufacturer passwords may be changed by writing a new password in Bytes 119-122 when the correct current fixed side manufacture password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.

6.2.11 Page Select

Byte 127 is used to select the upper page. A value of 00h indicates upper memory Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that upper Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, 20h and 21h indicate that the upper page identified is mapped to Bytes 128-255. If the host attempts to write a page select value which is not supported in a particular module, the Page Select byte will revert to 00h.

6.3 Upper Page 00h

Upper Page 00h consists of the Serial ID and is used for read only identification information.

TABLE 6-16 UPPER PAGE 00H MEMORY MAP

Byte	Size	Name	Description	PC	AC	AO	SM
128	1	Identifier	Identifier Type of free side device (See SFF-8024 Transceiver Management)	R	R	R	R
129	1	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability (See Table 6-17)	R	R	R	R
130	1	Connector Type	Code for media connector type (See SFF-8024 Transceiver Management)	R	R	R	R
131-138	8	Specification Compliance	Code for electronic or optical compatibility (See Table 6-18)	R	R	R	R
139	1	Encoding	Code for serial encoding algorithm. (See SFF-8024 Transceiver Management)	R	R	R	R
140	1	BR, nominal	Nominal bit rate, units of 100 Mbps. For BR > 25.4G, set this to FFh and use Byte 222.	R	R	R	R
141	1	Extended Rate Select Compliance	Tags for extended rate select compliance	R	R	R	R
142	1	Length (SMF)	Link length supported at the bit rate in byte 140 or page 00h byte 222, for SMF fiber in km *. A value of 1 shall be used for reaches from 0 to 1 km.	R	R	R	R
143	1	Length (OM3 50 um)	Link length supported at the bit rate in byte 140 or page 00h byte 222, for EBW 50/125 um fiber (OM3), units of 2 m *	R	R	R	R
144	1	Length (OM2 50 um)	Link length supported at the bit rate in byte 140 or page 00h byte 222, for 50/125 um fiber (OM2), units of 1 m *	R	R	R	R
145	1	Length (OM1 62.5 um) or Copper Cable Attenuation	Link length supported at the bit rate in byte 140 or page 00h byte 222, for 62.5/125 um fiber (OM1), units of 1 m *, or copper cable attenuation in dB at 25.78 GHz.	R	R	R	R
146	1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported at the bit rate in byte 140 or page 00h byte 222, for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147. See 6.3.12.	R	R	R	R
147	1	Device technology	Device technology (Table 6-19 and Table 6-20)	R	R	R	R
148-163	16	Vendor name	Free side device vendor name (ASCII)	R	R	R	R
164	1	Extended Module	Extended Module codes for InfiniBand (See Table 6-22)	R	R	R	R
165-167	3	Vendor OUI	Free side device vendor IEEE company ID	R	R	R	R
168-183	16	Vendor PN	Part number provided by free side device vendor(ASCII)	R	R	R	R
184-185	2	Vendor rev	Revision level for part number provided by vendor(ASCII)	R	R	R	R

Byte	Size	Name	Description	PC	AC	AO	SM
186-187	2	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)	R	R	R	R
188-189	2	Wavelength tolerance or Copper Cable Attenuation	Guaranteed range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)	R	R	R	R
190	1	Max case temp.	Maximum case temperature in degrees C	R	R	R	R
191	1	CC_BASE	Check code for base ID fields (Bytes 128-190)	R	R	R	R
192	1	Link codes	Extended Specification Compliance Codes (See SFF-8024 Transceiver Management)	R	R	R	R
193-195	3	Options	Rate Select, TX Disable, TX Fault, LOS, Warning indicators for: Temperature, VCC, RX power, TX Bias, TX EQ, Adaptive TX EQ, RX EMPH, CDR Bypass, CDR LOL Flag. See Table 6-23.	R	R	R	R
196-211	16	Vendor SN	Serial number provided by vendor (ASCII)	R	R	R	R
212-219	8	Date Code	Vendor's manufacturing date code	R	R	R	R
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved. See Table 6-25.	R	R	R	R
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device. See Table 6-26.	R	R	R	R
222	1	BR, nominal	Nominal bit rate per channel, units of 250 Mbps. Complements Byte 140. See Table 6-27.	R	R	R	R
223	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)	R	R	R	R
224-255	32	Vendor Specific	Vendor Specific EEPROM	-	-	-	-
* A value of zero means that the free side device does not support the specified technology or that the length information must be determined from the free side device technology.							

6.3.1 Identifier (00h 128)

The Identifier Values at Byte 128 specify the physical device described by the serial information. This value shall be included in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.2 Extended Identifier (00h 129)

The extended identifier provides additional information about the free side device. For example, the identifier indicates if the free side device contains a CDR function and identifies the power consumption class it belongs to.

New high power classes have been added to enable an emerging generation of capability requiring more than 3.5W of dissipation. However, legacy systems have generally been designed to a maximum of 3.5W. To ensure legacy systems are not harmed by power classes 5, 6 or 7 a lockout feature is added in Byte 93 bit 2 to enable them. A legacy system will not know about Byte 129 bits 1-0 or about Byte 93 bit 2. A new system will know about both and can configure power class 5 through 7 support accordingly. The power class identifiers specify maximum power dissipation over operating conditions and lifetime with all supported settings set to worst case values.

TABLE 6-17 EXTENDED IDENTIFIER VALUES (PAGE 00H BYTE 129)

Bit	Device Type
7-6	00: Power Class 1 (1.5 W max.)
	01: Power Class 2 (2.0 W max.)
	10: Power Class 3 (2.5 W max.)
	11: Power Class 4 (3.5 W max.)
5	Reserved
4	0: No CLEI code present in Page 02h
	1: CLEI code present in Page 02h
3	0: No CDR in TX, 1: CDR present in TX
2	0: No CDR in RX, 1: CDR present in RX
1-0	00: unused (legacy setting)
	01: Power Class 5 (4.0 W max.) See Byte 93 bit 2 to enable.
	10: Power Class 6 (4.5 W max.) See Byte 93 bit 2 to enable.
	11: Power Class 7 (5.0 W max.) See Byte 93 bit 2 to enable.

6.3.3 Connector Type (00h 130)

The Connector Type entry at Page 00H Byte 130 indicates the connector type for the separable portion of the free side device (see 4.3.2). This value shall be included in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.4 Specification Compliance (00h 131-138)

The bit significant indicators define the electronic or optical interfaces that are supported by the free side device. At least one bit shall be set in this field, and if more than one bit is applicable (as in the case of Fibre Channel), all shall be set accordingly. Except where stated, the interface supports 4 lanes of the standard.

TABLE 6-18 SPECIFICATION COMPLIANCE CODES (PAGE 00H BYTES 131-138)

Byte	Bit	Module Capability
		10/40G/100G Ethernet Compliance Codes
131	7	Extended: See section 6.3.23. The Extended Specification Compliance Codes are maintained in the Transceiver Management section of SFF-8024.
131	6	10GBASE-LRM
131	5	10GBASE-LR
131	4	10GBASE-SR
131	3	40GBASE-CR4
131	2	40GBASE-SR4
131	1	40GBASE-LR4
131	0	40G Active Cable (XLPPI)
		SONET Compliance Codes
132	7-3	Reserved
132	2	OC 48, long reach
132	1	OC 48, intermediate reach
132	0	OC 48 short reach
		SAS/SATA Compliance Codes
133	7	SAS 24.0 Gbps
133	6	SAS 12.0 Gbps
133	5	SAS 6.0 Gbps
133	4	SAS 3.0 Gbps
133	3-0	Reserved
		Gigabit Ethernet Compliance Codes
134	7-4	Reserved
134	3	1000BASE-T
134	2	1000BASE-CX
134	1	1000BASE-LX
134	0	1000BASE-SX
		Fibre Channel Link Length
135	7	Very long distance (V)
135	6	Short distance (S)
135	5	Intermediate distance (I)
135	4	Long distance (L)
135	3	Medium (M)
		Fibre Channel Transmitter Technology
135	2	Reserved
135	1	Longwave laser (LC)
135	0	Electrical inter-enclosure (EL)
136	7	Electrical intra-enclosure
136	6	Shortwave laser w/o OFC (SN)
136	5	Shortwave laser w OFC (SL)
136	4	Longwave Laser (LL)
136	3-0	Reserved

Byte	Bit	Module Capability
Fibre Channel Transmission Media		
137	7	Twin Axial Pair (TW)
137	6	Shielded Twisted Pair (TP)
137	5	Miniature Coax (MI)
137	4	Video Coax (TV)
137	3	Multi-mode 62.5 um (M6)
137	2	Multi-mode 50 um (M5)
137	1	Multi-mode 50 um (OM3)
137	0	Single Mode (SM)
Fibre Channel Speed		
138	7	1200 MBps (per channel)
138	6	800 MBps
138	5	1600 MBps (per channel)
138	4	400 MBps
138	3	3200 MBps (per channel)
138	2	200 MBps
138	1	Extended: See section 6.3.23. The Extended Specification Compliance Codes are maintained in the Transceiver Management section of SFF-8024.
138	0	100 MBps

6.3.5 Encoding (00h 139)

The Encoding Values at Page 00h Byte 139 indicate the serial encoding mechanism for the high-speed serial interface. The value shall be contained in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.6 Nominal Bit Rate (00h 140)

The nominal bit rate per channel (BR, nominal) is specified in units of 100 Megabits per second in Byte 140 and in units of 250 Megabits per second in Byte 222. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates the bit rate is not specified and must be determined from the Module technology. A value of FFh in Byte 140 means the bit rate exceeds 25.4Gb/s and Byte 222 must be used to determine nominal bit rate. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value (Byte 139).

6.3.7 Extended Rate Select Compliance (00h 141)

The Extended Rate Select Compliance field is used to allow a single free side device the flexibility to comply with single or multiple Extended Rate Select definitions. A definition is indicated by presence of a '1' in the specified bit. If exclusive, non-overlapping definitions are used, Page 00h Byte 141 will allow compliance to 8 distinct multi-rate definitions.

TABLE 6-19 EXTENDED RATE SELECT COMPLIANCE TAG ASSIGNMENT (PAGE 00H BYTE 141)

Byte	Bits	Description
141	7-2	Reserved
141	1-0	Rate Select Version. This functionality is different from SFF-8472 and SFF-8431. 10b: Rate Select Version 2 01b: Rate Select Version 1 00b, 11b: Reserved
Note: See 6.2.7 for further details of the use of this field		

6.3.8 Length (Standard SM Fiber) -km (00h 142)

In addition to EEPROM data from original GBIC definition, this value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using single mode fiber. Supported link length is as specified in INF-8074. The value is in units of kilometers. A value of zero means that the free side device does not support single mode fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables the value shall be zero.

6.3.9 Length (OM3) (00h 143)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50-micron multi-mode fiber. The value is in units of 2 meters. A value of zero means that the free side device does not support OM3 fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables the value shall be zero.

6.3.10 Length (OM2) (00h 144)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50-micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the free side device does not support OM2 fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables the value shall be zero.

6.3.11 Length (OM1) or Copper Cable Attenuation (00h 145)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 200 MHz*km (850 nm) and 500 MHz*km (1310 nm) 62.5-micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the free side device does not support OM1 fiber or that the length information must be determined from the free side device technology.

For copper cable assemblies, where page 00h byte 147 bits 7-4 are 1010b, 1011b, 1101b or 1111b, this register is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 25.78 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable. For active optical cables or copper cables not listed in this paragraph the value shall be zero.

6.3.12 Length: Cable Assembly or Optical Fiber (OM4) (00h 146)

If a separable module (as indicated by a value other than 23h in Byte 130) free side device transmitter technology is 850nm VCSEL (indicated by Byte 147 bits 7-4) then this value specifies the link length supported while operating in compliance with the applicable standards using 4700 MHz*km (850nm) extended bandwidth 50-micron multi-mode fiber (OM4). The value is in units of 2 meters.

Otherwise, this value specifies the link length of a Cable assembly (copper or AOC) in units of 1 meter. Link length is as specified in the INF-8074. Link lengths less than 1 meter shall indicate 1 meter.

A value of zero means the free side device is not a cable assembly or the length information must be determined from the separable free side device technology. A value of 255 means a separable module VCSEL free side device supports a link length greater than 508 meters or the cable assembly has a link length greater than 254 meters.

6.3.13 Device Technology (00h 147)

Aspects of the device or cable technology used are described by the Device Technology byte. An active optical cable may be distinguished from a separable module by reading Byte 130 (Connector Type).

TABLE 6-20 DEVICE TECHNOLOGY (PAGE 00H BYTE 147)

Bits	Description
7-4	Transmitter technology (See Table 6-21)
3	0: No wavelength control 1: Active wavelength control
2	0: Uncooled transmitter device 1: Cooled transmitter
1	0: Pin detector 1: APD detector
0	0: Transmitter not tunable 1: Transmitter tunable

TABLE 6-21 TRANSMITTER TECHNOLOGY (PAGE 00H BYTE 147 BITS 7-4)

Value	Description
0000b	850 nm VCSEL
0001b	1310 nm VCSEL
0010b	1550 nm VCSEL
0011b	1310 nm FP
0100b	1310 nm DFB
0101b	1550 nm DFB
0110b	1310 nm EML
0111b	1550 nm EML
1000b	Other / Undefined
1001b	1490 nm DFB
1010b	Copper cable unequalized
1011b	Copper cable passive equalized
1100b	Copper cable, near and far end limiting active equalizers
1101b	Copper cable, far end limiting active equalizers
1110b	Copper cable, near end limiting active equalizers
1111b	Copper cable, linear active equalizers

6.3.14 Vendor Name (00h 148-163)

The vendor name is a 16-character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

6.3.15 Extended Module Codes (00h 164)

The Extended Module Codes define the electronic or optical interfaces for InfiniBand that are supported by the free side device.

TABLE 6-22 EXTENDED MODULE CODE VALUES (PAGE 00H BYTE 164)

Byte	Bit	Module Code
InfiniBand Data Rate codes		
164	7-6	Reserved
	5	HDR
	4	EDR
	3	FDR
	2	QDR
	1	DDR
	0	SDR

6.3.16 Vendor Organizationally Unique Identifier Field (00h 165-167)

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

6.3.17 Vendor Part Number (00h 168-183)

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

6.3.18 Vendor Revision Number (00h 184-185)

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

6.3.19 Wavelength or Copper Cable Attenuation (00h 186-187)

For optical free side devices, this parameter identifies the nominal transmitter output wavelength at room temperature. This parameter is a 16-bit hex value with Byte 186 as high order byte and Byte 187 as low order byte. The laser wavelength is equal to the 16-bit integer value divided by 20 in nm (units of 0.05 nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected DWDM applications. For accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

If the free side device is identified as copper cable these registers will be used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

Byte 186 (00-FFh) is the copper cable attenuation at 2.5 GHz in units of 1 dB.

Byte 187 (00-FFh) is the copper cable attenuation at 5.0 GHz in units of 1 dB.

6.3.20 Wavelength Tolerance or Copper Cable Attenuation (00h 188-189)

The guaranteed +/- range of transmitter output wavelength under all normal operating conditions. For direct attach cable assemblies, the value is zero. This parameter is a 16-bit value with Byte 188 as high order byte and Byte 189 as low order byte. The laser wavelength is equal to the 16-bit integer value divided by 200 in nm (units of 0.005 nm). Thus, the following two examples:

Example 1:

10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in Bytes 186-187 = 1307.5 nm.
Represented as INT(1307.5 nm * 20) = 26150 = 6626h

Wavelength Tolerance in Bytes 188-189 = 47.5 nm.
Represented as INT(47.5 nm * 200) = 9500 = 251Ch

Example 2:

ITU-T Grid Wavelength = 1534.25 nm (195.4 THz) with 0.236 nm (30 GHz) Tolerance
Nominal Wavelength in Bytes 186-187 = 1534.25 nm.
Represented as INT(1534.25 nm * 20) = 30685 = 77DDh
Wavelength Tolerance in Bytes 188-189 = 0.236 nm.
Represented as INT(0.236 nm * 200) = 47 = 002Fh

If the free side device is identified as copper cable these registers will be used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

Byte 188 (00-FFh) is the copper cable attenuation at 7.0 GHz in units of 1 dB.

Byte 189 (00-FFh) is the copper cable attenuation at 12.9 GHz in units of 1 dB.

6.3.21 Maximum Case Temperature (00h 190)

This parameter allows specification of a maximum case temperature other than the standard 70C. Maximum case temperature is an 8-bit value in degrees C. A value of 00h indicates 70C.

6.3.22 CC_BASE (00h 191)

The check code is a 1-byte code that can be used to verify that the first 63 bytes of serial information in the free side device is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from 128 to 190, inclusive.

6.3.23 Extended Specification Compliance Codes (00h 192)

The Extended Specification Compliance Codes in Byte 192 identify the electronic or optical interfaces which are not included in Table 6-18 Specification Compliance Codes. These values are maintained in the Transceiver Management section of SFF-8024

6.3.24 Options (00h 193-195)

The bits in the option field shall specify the options implemented in the free side device.

Variable transceiver Tx input EQ and Rx output emphasis have been added, defined as the EQ and Emphasis capability designed into the transceiver in support of TP1a and TP4, respectively as defined in IEE802.3 Clause 86. Transceiver support of programmable EQ and Emphasis is found in Byte 193 bits 1 to 3 and shown below in Table 6-23. The default host control mechanism is "Fixed Position Programmable", found in Page 03h, Bytes 234-237 and documented in Table 6-33, Table 6-35 and Table 6-36. If a transceiver supports "Adaptive EQ", defined as transceiver automatic internal control of EQ position setting (without host intervention), it can be so identified in Byte 193 bit 3. Adaptive EQ algorithms and periodicity are implementation specific. Control of "Adaptive EQ" is done using Upper Page 03h Byte 241 bits 3-0 (per channel controls).

The magnitude of Tx input EQ and Rx output emphasis supported by the transceiver is identified in Page 03h Byte 224. This applies to either Fixed Position Programmable or Adaptive EQ modes.

CDR status and control functions are identified in Byte 194 bits 4 to 7. If Loss of Lock indicators (flags) are implemented bits 4 and 5 are set high. If CDR On/Off control is implemented bits 6 and 7 are set high. For transceivers with CDR capability, setting the CDR to ON engages the internal retiming function. Setting the CDR to OFF enables an internal bypassing mode, which directs traffic around the internal CDR. The two most common reasons to turn a CDR off (i.e. internally bypass it) are to run at bit rates not supported by a particular CDR or to save the thermal power in applications where CDR jitter mitigation is not required.

TABLE 6-23 OPTION VALUES (PAGE 00H BYTES 193-195)

Byte	Bit	Description	PC	AC	AO	SM
193	7-5	Reserved	-	-	-	-
	4	Tx Input Adaptive Equalizer Freeze Capable, coded 1 if implemented, else 0.	R	R	R	R
	3	TX Input Equalization Auto Adaptive Capable, coded 1 if implemented, else 0.	R	R	R	R
	2	TX Input Equalization Fixed Programmable Settings, coded 1 if implemented, else 0.	R	R	R	R
	1	RX Output Emphasis Fixed Programmable Settings, coded 1 if implemented, else 0.	R	R	R	R
	0	RX Output Amplitude Fixed Programmable Settings, coded 1 if implemented, else 0.	R	R	R	R
194	7	TX CDR On/Off Control implemented, (1b if controllable, 0b if fixed).	R	R	R	R
	6	RX CDR On/Off Control implemented, (1b if controllable, 0b if fixed).	R	R	R	R
	5	Tx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	R	R	R	R
	4	Rx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	R	R	R	R
	3	Rx Squelch Disable implemented, coded 1 if implemented, else 0.	R	R	R	R
	2	Rx Output Disable capable: coded 1 if implemented, else 0.	R	R	R	R
	1	Tx Squelch Disable implemented: coded 1 if implemented, else 0.	R	R	R	R
	0	Tx Squelch implemented: coded 1 if implemented, else 0.	R	R	R	R
195	7	Memory Page 02 provided: coded 1 if implemented, else 0.	R	R	R	R
	6	Memory Page 01h provided: coded 1 if implemented, else 0.	R	R	R	R
	5	Rate select is implemented as defined in 6.2.7. If the bit is set to 1 then refer to that section for multi-rate operation description.	C	C	C	C
	4	Tx_DISABLE is implemented and disables the serial output as defined by the relevant transmitter specification.	R	R	R	R
	3	Tx_FAULT signal implemented, coded 1 if implemented, else 0	R	R	R	R
	2	Tx Squelch implemented to reduce OMA coded 0, implemented to reduce Pave coded 1.	R	R	R	R
	1	Tx Loss of Signal implemented, coded 1 if implemented, else 0	R	R	R	R
	0	Pages 20-21h implemented. Default = 0 (not implemented).	R	R	R	R

6.3.25 Vendor Serial Number (00h 196-211)

The vendor serial number (vendor SN) is a 16-character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the free side device. A value of 0000h in the 16-byte field indicates that the vendor SN is unspecified.

6.3.26 Date Code (00h 212-219)

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory and shall be in the specified format.

TABLE 6-24 DATE CODES (PAGE 00H BYTES 212-219)

Byte	Description	PC	AC	AO	SM
212-213	ASCII code, two low order digits of year. (00=2000)	R	R	R	R
214-215	ASCII code digits of month (01=Jan through 12=Dec	R	R	R	R
216-217	ASCII code day of month (01-31)	R	R	R	R
218-219	ASCII code, Vendor Specific lot code, may be blank	R	R	R	R

6.3.27 Diagnostic Monitoring Type (00h 220)

'Diagnostic Monitoring Type' is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the free side device.

TABLE 6-25 DIAGNOSTIC MONITORING TYPE (PAGE 00H BYTE 220)

Byte	Bits	Description	PC	AC	AO	SM
220	7-6	Reserved	-	-	-	-
	5	Temperature monitoring implemented (0b=Not implemented or pre-Rev 2.8, 1b=Implemented)	R	R	R	R
	4	Supply voltage monitoring implemented (0b=Not implemented or pre-Rev 2.8, 1b=Implemented)	R	R	R	R
	3	Received power measurements type. 0=OMA 1=Average Power	R	R	R	R
	2	Transmitter power measurement. 0=Not supported 1=Supported	R	R	R	R
	1-0	Reserved	-	-	-	-

Digital Diagnostic Monitors monitor received power, bias current, supply voltage and temperature. Additionally, alarm and warning thresholds must be written as specified in this document. Auxiliary monitoring fields are optional extensions to Digital Diagnostics.

All digital monitoring values must be internally calibrated and reported in the units defined in 6.2.5.

Bit 2 indicates whether a transmitted power measurement is supported. The indication is required, however support of transmitter power measurement is optional (see Table 6-8). If the bit is set, transmitted power measurement is supported, and the module will monitor the average optical power. If not, transmitted power measurement is not supported.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. The indication is required, however support of received power measurement is optional (see Table 6-8). If the bit is set, average power is monitored. If not, received power measurement is not supported, or OMA is monitored.

6.3.28 Enhanced Options (00h 221)

See Table 6-26 for use of the Enhanced Options field. The state where the Rate Select declaration bits both have a value of 1 is reserved and should not be used.

TABLE 6-26 ENHANCED OPTIONS (PAGE 00H BYTE 221)

Byte	Bit	Description	PC	AC	AO	SM
221	7-5	Reserved	-	-	-	-
	4	Initialization Complete Flag implemented. This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at Byte 6 bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module.	R	R	R	R
	3	Rate Selection Declaration: When this Declaration bit is 0 the free side device does not support rate selection. When this Declaration bit is 1, rate selection is implemented using extended rate selection. See 6.2.7.2	R	R	R	R
	2	Application Select Table Declaration: When this Declaration bit is 1, the free side device supports rate selection using application select table mechanism. When this Declaration bit is 0, the free side device does not support application select and Page 01h does not exist. See 6.2.7.3	R	R	R	R
	1	TC readiness flag implemented. 0= TC readiness flag not implemented. 1= TC readiness flag is implemented.	R	R	R	R
	0	Reserved	-	-	-	-

To enable bit rates in excess of 25.4 Gbps, an extended bit rate field has been added in Byte 222 to supplement the existing values in Byte 140. The legacy Byte 140 contains bit rate at 100Mb/bit, which is limited to 25.4Gbps. The new Byte 222 contains bit rate at 250Mb/bit, enabling up to 63.5Gbps. A value of zero means this field is unspecified.

TABLE 6-27 EXTENDED BIT RATE: NOMINAL (PAGE 00H BYTE 222)

Byte	Bits	Description	PC	AC	AO	SM
222	7-0	Nominal bit rate, units of 250 Mbps. See Byte 140 description.	R	R	R	R

6.3.29 Check Code Extension (00h 223)

The check code is a 1-byte code that can be used to verify that the first 32 bytes of extended serial information in the free side device are valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from 192 to 222, inclusive.

6.3.30 Vendor Specific (00h 224-255)

This area may contain Vendor Specific information, which can be read from the free side device. The data is read only. Page 00h Bytes 224-255 may be used for Vendor Specific ID functions.

6.4 Upper Page 01h (Optional)

Page 01h is conditional on the state of bit 2 in Page 00h Byte 221.

TABLE 6-28 UPPER PAGE 01H APPLICATION SELECT TABLE (AST)

Byte	Bit	Name of Field	Description
128	7-0	CC_APPS	Check code for the AST: the check code shall be the low order bits of the sum of the contents of all the bytes from 129 to 255, inclusive.
129	7-6	Reserved	
129	5-0	AST Table Length, TL (length - 1)	A 6-bit binary number. TL, specifies the offset of the last application table entry defined in Bytes 130-255. TL is valid between 0 (1 entry) and 62 (for a total of 63 entries)
130,131	7-0,7-0	Application Code 0	Definition of first application supported (See Table 6-29)
Other Table Entries			
130+2*TL 131+2*TL	7-0, 7-0	Application code TL	Definition of last application supported (See Table 6-29)

Bytes 130-256 contain the application code table entries. Byte 129 bits 5-0 specify the number of entries in the table. Each application listed in the table requires two bytes.

TABLE 6-29 APPLICATION CODE STRUCTURE

Low Order Byte								High order Byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved		Category						Variant							

6.5 Upper Page 02h (Optional)

Page 02 is optionally provided as user writable EEPROM. The fixed side may read or write this memory for any purpose. If Page 00h Byte 129 bit 4 is set, however, the first 10 bytes of Page 02h Bytes 128-137 will be used to store the CLEI code for the free side device.

6.6 Upper Page 03h (Optional)

Upper Page 03h contains free side device thresholds, channel thresholds and masks, ability registers for optional equalizer, emphasis and amplitude,and optional channel controls. See 6.6.1, 6.6.3 and 6.6.4 for detailed descriptions of their use.

TABLE 6-30 UPPER PAGE 03H MEMORY MAP

Byte	# Bytes	Description	Type
128-175	48	Thresholds	Read-Only
176-223	48	Channel Thresholds	Read-Only
224	1	Tx EQ & Rx Emphasis Magnitude ID	Read-Only
225	1	RX output amplitude support indicators	Read-Only
226-241	16	Optional Channel Controls	Read/Write
242-251	10	Channel Monitor Masks	Read/Write
252-255	4	Reserved	Read/Write

6.6.1 Free Side Device and Channel Thresholds

Each monitor value has a corresponding high alarm, low alarm, high warning and low warning thresholds. For each monitor that is implemented, high and low alarm thresholds are required. These factory-preset values allow the user to determine when a particular value is outside of normal limits as determined by the free side device manufacturer. It is assumed that these values will vary with different technologies and different implementations. These values are stored in read-only memory in Page 03h Bytes 128-223.

TABLE 6-31 FREE SIDE DEVICE AND CHANNEL THRESHOLDS (PAGE 03H BYTES 128-223)

Byte	# Bytes	Name	Description	PC	AC	AO	SM
128-129	2	Temp High Alarm	MSB at lower byte address	C	C	C	C
130-131	2	Temp Low Alarm	MSB at lower byte address	C	C	C	C
132-133	2	Temp High Warning	MSB at lower byte address	O	O	O	O
134-135	2	Temp Low Warning	MSB at lower byte address	O	O	O	O
136-143	8	Reserved		-	-	-	-
144-145	2	Vcc High Alarm	MSB at lower byte address	C	C	C	C
146-147	2	Vcc Low Alarm	MSB at lower byte address	C	C	C	C
148-149	2	Vcc High Warning	MSB at lower byte address	O	O	O	O
150-151	2	Vcc Low Warning	MSB at lower byte address	O	O	O	O
152-159	8	Reserved		-	-	-	-
160-175	16	Vendor Specific		-	-	-	-
176-177	2	RX Power High Alarm	MSB at lower byte address	C	C	C	C
178-179	2	RX Power Low Alarm	MSB at lower byte address	C	C	C	C
180-181	2	RX Power High Warning	MSB at lower byte address	O	O	O	O
182-183	2	RX Power Low Warning	MSB at lower byte address	O	O	O	O
184-185	2	Tx Bias High Alarm	MSB at lower byte address	C	C	C	C
186-187	2	Tx Bias Low Alarm	MSB at lower byte address	C	C	C	C
188-189	2	Tx Bias High Warning	MSB at lower byte address	O	O	O	O
190-191	2	Tx Bias Low Warning	MSB at lower byte address	O	O	O	O
192-193	2	Tx Power High Alarm	MSB at lower byte address	C	C	C	C
194-195	2	Tx Power Low Alarm	MSB at lower byte address	C	C	C	C
196-197	2	Tx Power High Warning	MSB at lower byte address	O	O	O	O
198-199	2	Tx Power Low Warning	MSB at lower byte address	O	O	O	O

Byte	# Bytes	Name	Description	PC	AC	AO	SM
200-207	8	Reserved	Reserved thresholds for channel parameter set 4	-	-	-	-
208-215	8	Reserved	Reserved thresholds for channel parameter set 5	-	-	-	-
216-223	8	Vendor Specific		-	-	-	-

The values reported in the Alarm and Warning Thresholds area may be typical values at some chosen nominal operating conditions and may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is Vendor Specific and optional. Refer to the vendor's data sheet for use of alarm and warning thresholds.

6.6.2 Optional Equalizer, Emphasis and Amplitude Indicators

TABLE 6-32 EQUALIZER, EMPHASIS, AMPLITUDE AND TIMING (PAGE 03H BYTES 224-229)

Byte	Bit	Name	Description	PC	AC	AO	SM
224	7-4	Max Tx input equalization	Max Tx input equalization supported (controls are found in bytes 234-235 and codes are found in Table 6-35)	O	O	O	O
	3-0	Max Rx output emphasis	Max Rx output emphasis supported (controls are found in bytes 236-237 and codes are found in Table 6-36)	O	O	O	O
225	7-6	Reserved		-	-	-	-
	5-4	Rx output emphasis type	=00 Peak-to-peak amplitude stays constant, or not implemented, or no information =01 Steady state amplitude stays constant =10 Average of peak-to-peak and steady state amplitudes stays constant =11 Reserved	O	O	O	O
	3	RX output amplitude support	=0 Amplitude 0011 not supported or no information =1 Amplitude code 0011 Supported (See Table 6-34)	O	O	O	O
	2	RX output amplitude support	=0 Amplitude 0010 not supported or no information =1 Amplitude code 0010 Supported (See Table 6-34)	O	O	O	O
	1	RX output amplitude support	=0 Amplitude 0001 not supported or no information =1 Amplitude code 0001 Supported (See Table 6-34)	O	O	O	O
	0	RX output amplitude support	=0 Amplitude 0000 not supported or no information =1 Amplitude code 0000 Supported (See Table 6-34)	O	O	O	O
226-227	All	Reserved		-	-	-	-
228	All	Maximum TC stabilization time	Maximum time needed by the TC to reach its target working point under worst case conditions. LSB = 1 s.	O	O	O	O
229	All	Maximum CTLE settling time	Maximum time needed by CTLE adaptive algorithm to converge to an appropriate value under worst case conditions. LSB = 100 ms.	O	O	O	O

6.6.3 Optional Channel Controls

Upper Memory Page Control Bits are used to define the optional channel controls.

TABLE 6-33 OPTIONAL CHANNEL CONTROLS (PAGE 03H BYTES 230-241)

Byte	Bit	Name	Description	PC	AC	AO	SM
230-232	All	Reserved		-	-	-	-
233	7-4	Reserved		-	-	-	-
	3	Tx1AEFreeze	Tx Adaptive Equalization Freeze, channel 1. If supported (see page 00h byte 193 bit 4). Coded 1 to freeze, else 0.	0	0	0	0
	2	Tx2AEFreeze	Tx Adaptive Equalization Freeze, channel 2. If supported (see page 00h byte 193 bit 4). Coded 1 to freeze, else 0.	0	0	0	0
	1	Tx3AEFreeze	Tx Adaptive Equalization Freeze, channel 3. If supported (see page 00h byte 193 bit 4). Coded 1 to freeze, else 0.	0	0	0	0
	0	Tx4AEFreeze	Tx Adaptive Equalization Freeze, channel 4. If supported (see page 00h byte 193 bit 4). Coded 1 to freeze, else 0.	0	0	0	0
234	7-4	TX1 input equalization control	Input equalization control (see Page 03h Byte 224 and Table 6-35)	0	0	0	0
	3-0	TX2 input equalization control	Input equalization control (see Page 03h Byte 224 and Table 6-35)	0	0	0	0
235	7-4	TX3 input equalization control	Input equalization control (see Page 03h Byte 224 and Table 6-35)	0	0	0	0
	3-0	TX4 input equalization control	Input equalization control (see Page 03h Byte 224 and Table 6-35)	0	0	0	0
236	7-4	RX1 output emphasis control	Output emphasis control (see Page 03h Byte 224 and Table 6-36)	0	0	0	0
	3-0	RX2 output emphasis control	Output emphasis control (see Page 03h Byte 224 and Table 6-36)	0	0	0	0
237	7-4	RX3 output emphasis control	Output emphasis control (see Page 03h Byte 224 and Table 6-36)	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
	3-0	RX4 output emphasis control	Output emphasis control (see Page 03h Byte 224 and Table 6-36)	0	0	0	0
238	7-4	RX1 output amplitude control	Differential output amplitude without pre-emphasis. (See Table 6-34)	0	0	0	0
	3-0	RX2 output amplitude control	Differential output amplitude without pre-emphasis. (See Table 6-34)	0	0	0	0
239	7-4	RX3 output amplitude control	Differential output amplitude without pre-emphasis. (See Table 6-34)	0	0	0	0
	3-0	RX4 output amplitude control	Differential output amplitude without pre-emphasis. (See Table 6-34)	0	0	0	0
240	7	Rx4 SQ Disable	Rx Squelch Disable Channel 4 (optional)	0	0	0	0
	6	Rx3 SQ Disable	Rx Squelch Disable Channel 3 (optional)	0	0	0	0
	5	Rx2 SQ Disable	Rx Squelch Disable Channel 2 (optional)	0	0	0	0
	4	Rx1 SQ Disable	Rx Squelch Disable Channel 1 (optional)	0	0	0	0
	3	Tx4 SQ Disable	Tx Squelch Disable Channel 4 (optional)	0	0	0	0
	2	Tx3 SQ Disable	Tx Squelch Disable Channel 3 (optional)	0	0	0	0
	1	Tx2 SQ Disable	Tx Squelch Disable Channel 2 (optional)	0	0	0	0
	0	Tx1 SQ Disable	Tx Squelch Disable Channel 1 (optional)	0	0	0	0
241	7	Rx4 Output Disable	Rx Output Disable channel 4 (optional)	0	0	0	0
	6	Rx3 Output Disable	Rx Output Disable channel 3 (optional)	0	0	0	0
	5	Rx2 Output Disable	Rx Output Disable channel 2 (optional)	0	0	0	0
	4	Rx1 Output Disable	Rx Output Disable channel 1 (optional)	0	0	0	0
	3	TX4 adaptive equalization control	If implemented (see 00h 193 bit 3) 1b=Enable (default) 0b=Disable (use manual EQ)	-	-	-	-
	2	TX3 adaptive equalization control	If implemented (see 00h 193 bit 3) 1b=Enable (default) 0b=Disable (use manual EQ)	-	-	-	-
	1	TX2 adaptive equalization control	If implemented (see 00h 193 bit 3) 1b=Enable (default) 0b=Disable (use manual EQ)	-	-	-	-
	0	TX1 adaptive equalization control	If implemented (see 00h 193 bit 3) 1b=Enable (default) 0b=Disable (use manual EQ)	-	-	-	-

TABLE 6-34 OUTPUT DIFFERENTIAL AMPLITUDE CONTROL (PAGE 03H BYTES 238-239)

Value	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxxb	Reserved	
0111b	Reserved	mV(P-P)
0110b	Reserved	mV(P-P)
0101b	Reserved	mV(P-P)
0100b	Reserved	mV(P-P)
0011b	600-1200	mV(P-P)
0010b	400-800	mV(P-P)
0001b	300-600	mV(P-P)
0000b	100-400	mV(P-P)

TABLE 6-35 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

Value	Transmitter Input Equalization	
	Nominal	Units
11xxb	Reserved	
1011b	Reserved	
1010b	10	dB
1001b	9	dB
1000b	8	dB
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No EQ

TABLE 6-36 OUTPUT EMPHASIS CONTROL (PAGE 03H BYTES 236-237)

Value	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxxb	Reserved	
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No Emphasis

Output amplitude and output emphasis are defined at the appropriate test points defined by the relevant standard. There is an illustration of reference test points in SFF-8679.

Because receiver emphasis settings can affect receiver output amplitude (and vice versa) Table 6-34 and Table 6-36 define the variable parameter at a nominal condition of the other. For instance, Table 6-34 defines output amplitude at a zero output emphasis setting and Table 6-36 defines output emphasis at a nominal output amplitude setting (implementation dependent). The maximum emphasis supported is defined in section 6.6.2, Table 6-32 byte 224. If an implementation does not support all levels up to and including the maximum, the nearest value shall be used.

Squelch and output control functionality is optional. If implemented, squelch and output disable is controlled for each channel using Page 03h Bytes 240-241. Writing a '1' in the Squelch Disable register (Page 03h Byte 240) disables the squelch for the associated channel. Writing a '1' in the Output Disable register (Page 03h Byte 241) squelches the output of the associated channel. When a '1' is written in both registers for a channel, the associated output is disabled. The registers read all '0's upon power-up. All other squelch functionality details are outside the scope of this document.

6.6.4 Channel Monitor Masks

TABLE 6-37 CHANNEL MONITOR MASKS (PAGE 03H BYTES 242-251)

Byte	Bit	Name	Description	PC	AC	AO	SM
242	7	M-Rx1 Power High Alarm	Masking Bit for high RX Power alarm channel 1	C	C	C	C
	6	M-Rx1 Power Low Alarm	Masking Bit for low RX Power alarm channel 1	C	C	C	C
	5	M-Rx1 Power High Warning	Masking Bit for high RX Power warning channel 1	C	C	C	C
	4	M-Rx1 Power Low Warning	Masking Bit for low RX Power warning channel 1	C	C	C	C
	3	M-Rx2 Power High Alarm	Masking Bit for high RX Power alarm channel 2	C	C	C	C
	2	M-Rx2 Power Low Alarm	Masking Bit for low RX Power alarm channel 2	C	C	C	C
	1	M-Rx2 Power High Warning	Masking Bit for high RX Power warning channel 2	C	C	C	C
	0	M-Rx2 Power Low Warning	Masking Bit for low RX Power warning channel 2	C	C	C	C
243	7	M-Rx3 Power High Alarm	Masking Bit for high RX Power alarm channel 3	C	C	C	C
	6	M-Rx3 Power Low Alarm	Masking Bit for low RX Power alarm channel 3	C	C	C	C
	5	M-Rx3 Power High Warning	Masking Bit for high RX Power warning channel 3	C	C	C	C
	4	M-Rx3 Power Low Warning	Masking Bit for low RX Power warning channel 3	C	C	C	C
	3	M-Rx4 Power High Alarm	Masking Bit for high RX Power alarm channel 4	C	C	C	C
	2	M-Rx4 Power Low Alarm	Masking Bit for low RX Power alarm channel 4	C	C	C	C
	1	M-Rx4 Power High Warning	Masking Bit for high RX Power warning channel 4	C	C	C	C
	0	M-Rx4 Power Low Warning	Masking Bit for low RX Power warning channel 4	C	C	C	C
244	7	M-Tx1 Bias High Alarm	Masking Bit for high TX Bias alarm channel 1	C	C	C	C
	6	M-Tx1 Bias Low Alarm	Masking Bit for low TX Bias alarm channel 1	C	C	C	C
	5	M-Tx1 Bias High Warning	Masking Bit for high TX Bias warning channel 1	C	C	C	C
	4	M-Tx1 Bias Low Warning	Masking Bit for low TX Bias warning channel 1	C	C	C	C
	3	M-Tx2 Bias High Alarm	Masking Bit for high TX Bias alarm channel 2	C	C	C	C
	2	M-Tx2 Bias Low Alarm	Masking Bit for low TX Bias alarm channel 2	C	C	C	C
	1	M-Tx2 Bias High Warning	Masking Bit for high TX Bias warning channel 2	C	C	C	C
	0	M-Tx2 Bias Low Warning	Masking Bit for low TX Bias warning channel 2	C	C	C	C
245	7	M-Tx3 Bias High Alarm	Masking Bit for high TX Bias alarm channel 3	C	C	C	C
	6	M-Tx3 Bias Low Alarm	Masking Bit for low TX Bias alarm channel 3	C	C	C	C

Byte	Bit	Name	Description	PC	AC	AO	SM
	5	M-Tx3 Bias High Warning	Masking Bit for high TX Bias warning channel 3	C	C	C	C
	4	M-Tx3 Bias Low Warning	Masking Bit for low TX Bias warning channel 3	C	C	C	C
	3	M-Tx4 Bias High Alarm	Masking Bit for high TX Bias alarm channel 4	C	C	C	C
	2	M-Tx4 Bias Low Alarm	Masking Bit for low TX Bias alarm channel 4	C	C	C	C
	1	M-Tx4 Bias High Warning	Masking Bit for high TX Bias warning channel 4	C	C	C	C
	0	M-Tx4 Bias Low Warning	Masking Bit for low TX Bias warning channel 4	C	C	C	C
246	7	M-Tx1 Power High Alarm	Masking Bit for high TX Power alarm channel 1	C	C	C	C
	6	M-Tx1 Power Low Alarm	Masking Bit for low TX Power alarm channel 1	C	C	C	C
	5	M-Tx1 Power High Warning	Masking Bit for high TX Power warning channel 1	C	C	C	C
	4	M-Tx1 Power Low Warning	Masking Bit for low TX Power warning channel 1	C	C	C	C
	3	M-Tx2 Power High Alarm	Masking Bit for high TX Power alarm channel 2	C	C	C	C
	2	M-Tx2 Power Low Alarm	Masking Bit for low TX Power alarm channel 2	C	C	C	C
	1	M-Tx2 Power High Warning	Masking Bit for high TX Power warning channel 2	C	C	C	C
	0	M-Tx2 Power Low Warning	Masking Bit for low TX Power warning channel 2	C	C	C	C
247	7	M-Tx3 Power High Alarm	Masking Bit for high TX Power alarm channel 3	C	C	C	C
	6	M-Tx3 Power Low Alarm	Masking Bit for low TX Power alarm channel 3	C	C	C	C
	5	M-Tx3 Power High Warning	Masking Bit for high TX Power warning channel 3	C	C	C	C
	4	M-Tx3 Power Low Warning	Masking Bit for low TX Power warning channel 3	C	C	C	C
	3	M-Tx4 Power High Alarm	Masking Bit for high TX Power alarm channel 4	C	C	C	C
	2	M-Tx4 Power Low Alarm	Masking Bit for low TX Power alarm channel 4	C	C	C	C
	1	M-Tx4 Power High Warning	Masking Bit for high TX Power warning channel 4	C	C	C	C
	0	M-Tx4 Power Low Warning	Masking Bit for low TX Power warning channel 4	C	C	C	C
248-249	All	Reserved	Reserved channel monitor masks set 4	-	-	-	-
250-251	All	Reserved	Reserved channel monitor masks set 5	-	-	-	-

6.7 Upper Page 20h and Upper Page 21h (Optional)

The Upper Page 20h and Upper Page 21h contain support for additional monitored parameters for modules that have PAM4 modulation and/or have optical transmission wavelengths on a DWDM grid.

6.7.1 Overview

Many additional parameters may be supported by a QSFP with advanced modulation techniques. To allow monitoring of these parameters two new pages in the SFF-8436/SFF-8636 memory space are utilized. Pages 20h and 21h are assigned to monitor these parameters. The basic monitoring techniques are the same as for other monitored parameters (i.e., they support current value, latched warning/alarm status, masks and thresholds). To indicate to the host device whether pages 20h and 21h are supported, page 00h byte 195 bit 0 is used. A value of 1b indicates that page 20h and 21h are supported as described in this section. A value of 0b indicates that pages 20h and 21h are not supported by the module.

For a PAM4 signal several additional parameters are very useful to determine the health of the module and the line environment. These include bit error ratio and frame error rate calculations, a signal-to-noise ratio measurement and a level transition measurement that characterize the PAM eye, and a residual dispersion measurement.

For a module implementing a Dense Wavelength Division Multiplexing optical interface, there is a significant benefit in providing access to additional diagnostic monitoring parameters specifically for a DWDM module. In DWDM the wavelength or frequency of the laser is an extremely important parameter and monitoring it allows the health of the laser to be known. When a direct measurement of the error in the frequency is not available, the laser temperature deviation from target is often used as a proxy. In addition, DWDM modules typically use a thermo-electric cooler (TEC) to control the laser temperature. The current flowing through the TEC is a strong indicator of the health of the module. A warning or error indication in any of these parameters can be an early indication of pending module failure.

Other modules may require additional parameters to be defined in the future.

It is expected that not all possible features will be supported by all modules or on all channels. To address this situation, this specification allows the module to determine which parameters are being monitored. Some parameters may be module-level in scope, and some may be channel-specific. This information is conveyed by the module to the host in the 2-byte parameter configuration registers (page 20h bytes 200-248). To indicate that one or more parameters are not supported the module will report 00h in both bytes of the configuration register for that parameter.

Up to 24 different parameters can be monitored, each providing a real-time value as well as alarm and warning flags. 16 threshold value sets are provided, and each of the 24 parameters is associated by the module with one of the threshold value sets. The parameter configuration registers indicate which threshold set is to be used with each parameter. Note that this implies that multiple parameters may share the same threshold set (for example, if the same parameter is measured on multiple channels).

To facilitate future functionality without major specification changes, the parameter configuration registers provide an enumerated value for the specific parameter to be monitored.

In addition to parameter monitoring, this specification includes a read-only logical mapping indication feature which associates electrical channels with optical channels when that mapping is defined.

6.7.2 Registers for Page 20h and 21h

6.7.2.1 Overview

TABLE 6-38 REGISTER OVERVIEW FOR PAGE 20H

Byte	Size	Name	Description	PC	AC	AO	SM
128-139	12	Param Alarms	Latched alarm/warning flags for monitored parameters (see 6.7.2.2)	0	0	0	0
140-151	12	Param Masks	Interrupt mask values for monitored parameters (see 6.7.2.3)	0	0	0	0
152-199	48	Param Values	Real-time values for monitored parameters (see 6.7.2.4)	0	0	0	0
200-247	48	Param Configuration	Parameter configuration registers (see 6.7.2.5)	0	0	0	0
248-249	2	Lane mapping	Lane mapping (see 6.7.2.6)	0	0	0	0
250-255	6	Other configuration	Error counter reset and other configurations (see 6.7.2.7)	0	0	0	0

TABLE 6-39 REGISTER OVERVIEW FOR PAGE 21H

Byte	Size	Name	Description	PC	AC	AO	SM
128-255	128	Param Thresholds	Parameter alarm and warning thresholds (page 21h, see 6.7.2.8)	0	0	0	0

6.7.2.2 Latched Alarm/Warning Flags for Monitored Parameters

These 12 bytes cover the latched alarm and warning flags for the monitored parameters specified by the parameter configuration registers. Each parameter has 4 bits with the most-significant bit representing the alarm high error, followed by alarm low, warning high and warning low as with other alarm and warning flags. Note that the threshold against which the real-time value is compared to generate these alarms and warnings is specified in the Parameter Configuration Registers.

TABLE 6-40 LATCHED ALARM/WARNING FLAGS (PAGE 20H BYTES 128-139)

Byte	Bit	Name	Description	PC	AC	AO	SM
128	7-4	L-Param1 Alarm/Warning	Latched alarm/warning flags for monitored parameter 1	0	0	0	0
	3-0	L-Param2 Alarm/Warning	Latched alarm/warning flags for monitored parameter 2	0	0	0	0
129	7-4	L-Param3 Alarm/Warning	Latched alarm/warning flags for monitored parameter 3	0	0	0	0
	3-0	L-Param4 Alarm/Warning	Latched alarm/warning flags for monitored parameter 4	0	0	0	0
130	7-4	L-Param5 Alarm/Warning	Latched alarm/warning flags for monitored parameter 5	0	0	0	0
	3-0	L-Param6 Alarm/Warning	Latched alarm/warning flags for monitored parameter 6	0	0	0	0
131	7-4	L-Param7 Alarm/Warning	Latched alarm/warning flags for monitored parameter 7	0	0	0	0
	3-0	L-Param8 Alarm/Warning	Latched alarm/warning flags for monitored parameter 8	0	0	0	0
132	7-4	L-Param9 Alarm/Warning	Latched alarm/warning flags for monitored parameter 9	0	0	0	0
	3-0	L-Param10 Alarm/Warning	Latched alarm/warning flags for monitored parameter 10	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
133	7-4	L-Param11 Alarm/Warning	Latched alarm/warning flags for monitored parameter 11	0	0	0	0
	3-0	L-Param12 Alarm/Warning	Latched alarm/warning flags for monitored parameter 12	0	0	0	0
134	7-4	L-Param13 Alarm/Warning	Latched alarm/warning flags for monitored parameter 13	0	0	0	0
	3-0	L-Param14 Alarm/Warning	Latched alarm/warning flags for monitored parameter 14	0	0	0	0
135	7-4	L-Param15 Alarm/Warning	Latched alarm/warning flags for monitored parameter 15	0	0	0	0
	3-0	L-Param16 Alarm/Warning	Latched alarm/warning flags for monitored parameter 16	0	0	0	0
136	7-4	L-Param17 Alarm/Warning	Latched alarm/warning flags for monitored parameter 17	0	0	0	0
	3-0	L-Param18 Alarm/Warning	Latched alarm/warning flags for monitored parameter 18	0	0	0	0
137	7-4	L-Param19 Alarm/Warning	Latched alarm/warning flags for monitored parameter 19	0	0	0	0
	3-0	L-Param20 Alarm/Warning	Latched alarm/warning flags for monitored parameter 20	0	0	0	0
138	7-4	L-Param21 Alarm/Warning	Latched alarm/warning flags for monitored parameter 21	0	0	0	0
	3-0	L-Param22 Alarm/Warning	Latched alarm/warning flags for monitored parameter 22	0	0	0	0
139	7-4	L-Param23 Alarm/Warning	Latched alarm/warning flags for monitored parameter 23	0	0	0	0
	3-0	L-Param24 Alarm/Warning	Latched alarm/warning flags for monitored parameter 24	0	0	0	0

6.7.2.3 Mask Registers for Monitored Parameters

These 12 bytes cover the interrupt masks for the latched alarm and warning flags. Each parameter has 4 bits with the most-significant bit representing the alarm high error, followed by low alarm, high warning and low warning as with other alarm and warning parameters. When a particular bit is 0, then the corresponding flag generates an interrupt. If the bit is 1 then an interrupt is not generated. As with the alarm and warning flags, for each parameter the highest bit number represents alarm high followed by alarm low, warning high and warning low masks.

TABLE 6-41 INTERRUPT MASK REGISTERS (PAGE 20H BYTES 140-151)

Byte	Bit	Name	Description	PC	AC	AO	SM
140	7-4	M-Param1 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 1	0	0	0	0
	3-0	M-Param2 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 2	0	0	0	0
141	7-4	M-Param3 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 3	0	0	0	0
	3-0	M-Param4 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 4	0	0	0	0
142	7-4	M-Param5 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 5	0	0	0	0
	3-0	M-Param6 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 6	0	0	0	0
143	7-4	M-Param7 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 7	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
	3-0	M-Param8 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 8	0	0	0	0
144	7-4	M-Param9 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 9	0	0	0	0
	3-0	M-Param10 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 10	0	0	0	0
145	7-4	M-Param11 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 11	0	0	0	0
	3-0	M-Param12 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 12	0	0	0	0
146	7-4	M-Param13 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 13	0	0	0	0
	3-0	M-Param14 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 14	0	0	0	0
147	7-4	M-Param15 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 15	0	0	0	0
	3-0	M-Param16 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 16	0	0	0	0
148	7-4	M-Param17 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 17	0	0	0	0
	3-0	M-Param18 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 18	0	0	0	0
149	7-4	M-Param19 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 19	0	0	0	0
	3-0	M-Param20 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 20	0	0	0	0
150	7-4	M-Param21 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 21	0	0	0	0
	3-0	M-Param22 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 22	0	0	0	0
151	7-4	M-Param23 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 23	0	0	0	0
	3-0	M-Param24 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 24	0	0	0	0

6.7.2.4 Real-Time Value of Monitored Parameters

These 48 bytes contain the real-time value of the monitored parameters. They are to be interpreted as specified in the Parameter Configuration Registers. In addition, the module will compare these values to the corresponding thresholds indicated in the Parameter Configuration Registers to generate the appropriate alarms and/or warnings in the registers above. As with the rest of SFF-8636, these parameters are all stored with the most significant byte in the lower numbered address.

TABLE 6-42 REAL-TIME VALUE REGISTERS (PAGE 20H BYTES 152-199)

Byte	Bit	Name	Description	PC	AC	AO	SM
152	All	Param 1 MSB	Real-time value of parameter 1 (MSB)	0	0	0	0
153	All	Param 1 LSB	Real-time value of parameter 1 (LSB)	0	0	0	0
154	All	Param 2 MSB	Real-time value of parameter 2 (MSB)	0	0	0	0
155	All	Param 2 LSB	Real-time value of parameter 2 (LSB)	0	0	0	0
156	All	Param 3 MSB	Real-time value of parameter 3 (MSB)	0	0	0	0
157	All	Param 3 LSB	Real-time value of parameter 3 (LSB)	0	0	0	0
158	All	Param 4 MSB	Real-time value of parameter 4 (MSB)	0	0	0	0
159	All	Param 4 LSB	Real-time value of parameter 4 (LSB)	0	0	0	0
160	All	Param 5 MSB	Real-time value of parameter 5 (MSB)	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
161	All	Param 5 LSB	Real-time value of parameter 5 (LSB)	0	0	0	0
162	All	Param 6 MSB	Real-time value of parameter 6 (MSB)	0	0	0	0
163	All	Param 6 LSB	Real-time value of parameter 6 (LSB)	0	0	0	0
164	All	Param 7 MSB	Real-time value of parameter 7 (MSB)	0	0	0	0
165	All	Param 7 LSB	Real-time value of parameter 7 (LSB)	0	0	0	0
166	All	Param 8 MSB	Real-time value of parameter 8 (MSB)	0	0	0	0
167	All	Param 8 LSB	Real-time value of parameter 8 (LSB)	0	0	0	0
168	All	Param 9 MSB	Real-time value of parameter 9 (MSB)	0	0	0	0
169	All	Param 9 LSB	Real-time value of parameter 9 (LSB)	0	0	0	0
170	All	Param 10 MSB	Real-time value of parameter 10 (MSB)	0	0	0	0
171	All	Param 10 LSB	Real-time value of parameter 10 (LSB)	0	0	0	0
172	All	Param 11 MSB	Real-time value of parameter 11 (MSB)	0	0	0	0
173	All	Param 11 LSB	Real-time value of parameter 11 (LSB)	0	0	0	0
174	All	Param 12 MSB	Real-time value of parameter 12 (MSB)	0	0	0	0
175	All	Param 12 LSB	Real-time value of parameter 12 (LSB)	0	0	0	0
176	All	Param 13 MSB	Real-time value of parameter 13 (MSB)	0	0	0	0
177	All	Param 13 LSB	Real-time value of parameter 13 (LSB)	0	0	0	0
178	All	Param 14 MSB	Real-time value of parameter 14 (MSB)	0	0	0	0
179	All	Param 14 LSB	Real-time value of parameter 14 (LSB)	0	0	0	0
180	All	Param 15 MSB	Real-time value of parameter 15 (MSB)	0	0	0	0
181	All	Param 15 LSB	Real-time value of parameter 15 (LSB)	0	0	0	0
182	All	Param 16 MSB	Real-time value of parameter 16 (MSB)	0	0	0	0
183	All	Param 16 LSB	Real-time value of parameter 16 (LSB)	0	0	0	0
184	All	Param 17 MSB	Real-time value of parameter 17 (MSB)	0	0	0	0
185	All	Param 17 LSB	Real-time value of parameter 17 (LSB)	0	0	0	0
186	All	Param 18 MSB	Real-time value of parameter 18 (MSB)	0	0	0	0
187	All	Param 18 LSB	Real-time value of parameter 18 (LSB)	0	0	0	0
188	All	Param 19 MSB	Real-time value of parameter 19 (MSB)	0	0	0	0
189	All	Param 19 LSB	Real-time value of parameter 19 (LSB)	0	0	0	0
190	All	Param 20 MSB	Real-time value of parameter 20 (MSB)	0	0	0	0
191	All	Param 20 LSB	Real-time value of parameter 20 (LSB)	0	0	0	0
192	All	Param 21 MSB	Real-time value of parameter 21 (MSB)	0	0	0	0
193	All	Param 21 LSB	Real-time value of parameter 21 (LSB)	0	0	0	0
194	All	Param 22 MSB	Real-time value of parameter 22 (MSB)	0	0	0	0
195	All	Param 22 LSB	Real-time value of parameter 22 (LSB)	0	0	0	0
196	All	Param 23 MSB	Real-time value of parameter 23 (MSB)	0	0	0	0
197	All	Param 23 LSB	Real-time value of parameter 23 (LSB)	0	0	0	0
198	All	Param 24 MSB	Real-time value of parameter 24 (MSB)	0	0	0	0
199	All	Param 24 LSB	Real-time value of parameter 24 (LSB)	0	0	0	0

6.7.2.5 Parameter Configuration Registers

These 48 bytes determine how the real-time value registers, alarms and warnings, masks and thresholds are to be interpreted by the host. For each of the 24 possible monitored parameters the monitoring point, parameter type and threshold location are provided by the module. The parameter configuration is a 2-byte field which is described below.

TABLE 6-43 PARAMETER CONFIGURATION REGISTERS (PAGE 20H BYTES 200-247)

Byte	Bit	Name	Description	PC	AC	AO	SM
200	All	Config 1 MSB	Configuration for parameter 1 (MSB)	0	0	0	0
201	All	Config 1 LSB	Configuration for parameter 1 (LSB)	0	0	0	0
202	All	Config 2 MSB	Configuration for parameter 2 (MSB)	0	0	0	0
203	All	Config 2 LSB	Configuration for parameter 2 (LSB)	0	0	0	0
204	All	Config 3 MSB	Configuration for parameter 3 (MSB)	0	0	0	0

Byte	Bit	Name	Description	PC	AC	AO	SM
205	All	Config 3 LSB	Configuration for parameter 3 (LSB)	0	0	0	0
206	All	Config 4 MSB	Configuration for parameter 4 (MSB)	0	0	0	0
207	All	Config 4 LSB	Configuration for parameter 4 (LSB)	0	0	0	0
208	All	Config 5 MSB	Configuration for parameter 5 (MSB)	0	0	0	0
209	All	Config 5 LSB	Configuration for parameter 5 (LSB)	0	0	0	0
210	All	Config 6 MSB	Configuration for parameter 6 (MSB)	0	0	0	0
211	All	Config 6 LSB	Configuration for parameter 6 (LSB)	0	0	0	0
212	All	Config 7 MSB	Configuration for parameter 7 (MSB)	0	0	0	0
213	All	Config 7 LSB	Configuration for parameter 7 (LSB)	0	0	0	0
214	All	Config 8 MSB	Configuration for parameter 8 (MSB)	0	0	0	0
215	All	Config 8 LSB	Configuration for parameter 8 (LSB)	0	0	0	0
216	All	Config 9 MSB	Configuration for parameter 9 (MSB)	0	0	0	0
217	All	Config 9 LSB	Configuration for parameter 9 (LSB)	0	0	0	0
218	All	Config 10 MSB	Configuration for parameter 10 (MSB)	0	0	0	0
219	All	Config 10 LSB	Configuration for parameter 10 (LSB)	0	0	0	0
220	All	Config 11 MSB	Configuration for parameter 11 (MSB)	0	0	0	0
221	All	Config 11 LSB	Configuration for parameter 11 (LSB)	0	0	0	0
222	All	Config 12 MSB	Configuration for parameter 12 (MSB)	0	0	0	0
223	All	Config 12 LSB	Configuration for parameter 12 (LSB)	0	0	0	0
224	All	Config 13 MSB	Configuration for parameter 13 (MSB)	0	0	0	0
225	All	Config 13 LSB	Configuration for parameter 13 (LSB)	0	0	0	0
226	All	Config 14 MSB	Configuration for parameter 14 (MSB)	0	0	0	0
227	All	Config 14 LSB	Configuration for parameter 14 (LSB)	0	0	0	0
228	All	Config 15 MSB	Configuration for parameter 15 (MSB)	0	0	0	0
229	All	Config 15 LSB	Configuration for parameter 15 (LSB)	0	0	0	0
230	All	Config 16 MSB	Configuration for parameter 16 (MSB)	0	0	0	0
231	All	Config 16 LSB	Configuration for parameter 16 (LSB)	0	0	0	0
232	All	Config 17 MSB	Configuration for parameter 17 (MSB)	0	0	0	0
233	All	Config 17 LSB	Configuration for parameter 17 (LSB)	0	0	0	0
234	All	Config 18 MSB	Configuration for parameter 18 (MSB)	0	0	0	0
235	All	Config 18 LSB	Configuration for parameter 18 (LSB)	0	0	0	0
236	All	Config 19 MSB	Configuration for parameter 19 (MSB)	0	0	0	0
237	All	Config 19 LSB	Configuration for parameter 19 (LSB)	0	0	0	0
238	All	Config 20 MSB	Configuration for parameter 20 (MSB)	0	0	0	0
239	All	Config 20 LSB	Configuration for parameter 20 (LSB)	0	0	0	0
240	All	Config 21 MSB	Configuration for parameter 21 (MSB)	0	0	0	0
241	All	Config 21 LSB	Configuration for parameter 21 (LSB)	0	0	0	0
242	All	Config 22 MSB	Configuration for parameter 22 (MSB)	0	0	0	0
243	All	Config 22 LSB	Configuration for parameter 22 (LSB)	0	0	0	0
244	All	Config 23 MSB	Configuration for parameter 23 (MSB)	0	0	0	0
245	All	Config 23 LSB	Configuration for parameter 23 (LSB)	0	0	0	0
246	All	Config 24 MSB	Configuration for parameter 24 (MSB)	0	0	0	0
247	All	Config 24 LSB	Configuration for parameter 24 (LSB)	0	0	0	0

The two bytes of parameter are stored most significant byte-first with the following definition:

TABLE 6-44 PARAMETER CONFIGURATION DETAILS

Byte	Bits	Description
MSB	7:4	Threshold ID. This number corresponds to which threshold set (1-16) will be used for this parameter.
	3	Reserved
	2	Parameter monitored at: 0b = Global module 1b = Channel-specific (see bits 1:0)
	1:0	Channel number, if the parameter is monitored channel-specific, per bit 2.
LSB	7:0	Parameter type (see Table 6-45)

The parameter type value is taken from the following table:

TABLE 6-45 PARAMETER TYPE ENUMERATION

Value	Description
0	Parameter not supported. This value means that the module is not presenting any data on the corresponding real-time value, or latched flag registers.
1	SNR, line ingress (see section 6.7.4.1)
2	Residual ISI/Dispersion, line ingress (see section 6.7.4.2)
3	PAM4 Level Transition Parameter, line ingress (see section 6.7.4.3)
4	Pre-FEC BER, average, line ingress (see section 6.7.4.4)
5	FER, average, line ingress (see section 6.7.4.4)
6	TEC Current (see section 6.7.5.1)
7	Laser Frequency (see section 6.7.5.2)
8	Laser Temperature (see section 6.7.5.3)
9	Pre-FEC BER, latched minimum value since last read, line ingress (see section 6.7.4.4)
10	Pre-FEC BER, latched maximum value since last read, line ingress (see section 6.7.4.4)
11	Pre-FEC BER, prior period, line ingress (see section 6.7.4.4)
12	Pre-FEC BER, current, line ingress (see section 6.7.4.4)
13	FER, latched minimum value since last read, line ingress (see section 6.7.4.4)
14	FER, latched maximum value since last read, line ingress (see section 6.7.4.4)
15	FER, prior period, line ingress (see section 6.7.4.4)
16	FER, current, line ingress (see section 6.7.4.4)
17-191	Reserved
192-255	Vendor-specific

6.7.2.6 Electrical/Optical Lane Mapping

This read-only feature allows the host to retrieve the electrical to optical channel mapping. For a PAM4 encoding, the electrical channel can be either mapped to the MSB or the LSB of the optical channel. This parameter is read-only. Each electrical channel has a 4-bit register in register 183 or 184 to define this mapping:

TABLE 6-46 LANE MAPPING REGISTERS (TABLE 20H BYTES 248-249)

Byte	Bit	Name	Description	PC	AC	AO	SM
248	7-4	Mapping Lane 1	Line side mapping for electrical channel 1 (see Table 6-47)	O	O	O	O
	3-0	Mapping Lane 2	Line side mapping for electrical channel 2 (see Table 6-47)	O	O	O	O
249	7-4	Mapping Lane 3	Line side mapping for electrical channel 3 (see Table 6-47)	O	O	O	O
	3-0	Mapping Lane 4	Line side mapping for electrical channel 4 (see Table 6-47)	O	O	O	O

And the mapping is defined in Table 6-47.

TABLE 6-47 LANE MAPPING ENUMERATION

Value	Description
0	Not determined or not supported. This means that the data from the electrical lane could be spread amongst any optical lane and between LSB and MSB. This may be the case for example, in FEC encoded data or gray mapped data. Use this value also to mean that lane mapping is not supported.
1	Optical Lane 1, LSB. This means that all of the data from the electrical lane appears on optical lane 1 in the LSB.
2	Optical Lane 1, MSB. This means that all of the data from the electrical lane appears on optical lane 1 in the MSB.
3	Optical Lane 2, LSB. This means that all of the data from the electrical lane appears on optical lane 2 in the LSB.
4	Optical Lane 2, MSB. This means that all of the data from the electrical lane appears on optical lane 2 in the MSB.
5	Optical Lane 1. This means that all of the data from the electrical lane appears on optical lane 1, but it might be LSB or MSB or spread between the two based on encoding.
6	Optical Lane 2. This means that all of the data from the electrical lane appears on optical lane 2, but it might be LSB or MSB or spread between the two based on encoding.
7-12	Reserved
13-15	Vendor specific mapping

6.7.2.7 Other Configuration Registers

This section contains a single bit that enables the host to reset the module error counters so that a recent BER can be presented. Other bits and registers are reserved.

TABLE 6-48 OTHER CONFIGURATION REGISTERS (TABLE 20H BYTES 250-255)

Byte	Bit	Name	Description	PC	AC	AO	SM
250	7	Error Reset	1b = Reset error counters (clears back to zero automatically when the counters have been reset)	O	O	O	O
	6-0	Reserved	Reserved	-	-	-	-
251-255	All	Reserved	Reserved	-	-	-	-

6.7.2.8 Threshold Registers

This section contains the 16 threshold register sets against which the various parameters will be compared to determine if an alarm or warning flag should be generated. Each threshold set has 4 2-Byte registers ordered most significant byte-first, and the registers are in the same order as other threshold registers in SFF-8636: alarm high threshold, alarm low threshold, warning high threshold, warning low threshold. The units of the threshold values are identified by the corresponding parameter value which is assigned to the threshold set.

TABLE 6-49 THRESHOLD REGISTERS (PAGE 21H BYTES 128-255)

Byte	Bit	Name	Description	PC	AC	AO	SM
128-135	All	Param Threshold Set 1	Threshold set 1, same order as other SFF-8636 threshold sets	O	O	O	O
136-143	All	Param Threshold Set 2	Threshold set 2, same order as other SFF-8636 threshold sets	O	O	O	O
144-151	All	Param Threshold Set 3	Threshold set 3, same order as other SFF-8636 threshold sets	O	O	O	O
152-159	All	Param Threshold Set 4	Threshold set 4, same order as other SFF-8636 threshold sets	O	O	O	O
160-167	All	Param Threshold Set 5	Threshold set 5, same order as other SFF-8636 threshold sets	O	O	O	O
168-175	All	Param Threshold Set 6	Threshold set 6, same order as other SFF-8636 threshold sets	O	O	O	O
176-183	All	Param Threshold Set 7	Threshold set 7, same order as other SFF-8636 threshold sets	O	O	O	O
184-191	All	Param Threshold Set 8	Threshold set 8, same order as other SFF-8636 threshold sets	O	O	O	O
192-199	All	Param Threshold Set 9	Threshold set 9, same order as other SFF-8636 threshold sets	O	O	O	O
200-207	All	Param Threshold Set 10	Threshold set 10, same order as other SFF-8636 threshold sets	O	O	O	O
208-215	All	Param Threshold Set 11	Threshold set 11, same order as other SFF-8636 threshold sets	O	O	O	O
216-223	All	Param Threshold Set 12	Threshold set 12, same order as other SFF-8636 threshold sets	O	O	O	O
224-231	All	Param Threshold Set 13	Threshold set 13, same order as other SFF-8636 threshold sets	O	O	O	O
232-239	All	Param Threshold Set 14	Threshold set 14, same order as other SFF-8636 threshold sets	O	O	O	O
240-247	All	Param Threshold Set 15	Threshold set 15, same order as other SFF-8636 threshold sets	O	O	O	O
248-255	All	Param Threshold Set 16	Threshold set 16, same order as other SFF-8636 threshold sets	O	O	O	O

6.7.3 Diagrams for PAM4 Monitored Parameters

Figure 6-2 below shows a general block diagram of the optical ingress path of a module showing the location where the SNR and level transition parameters are measured.

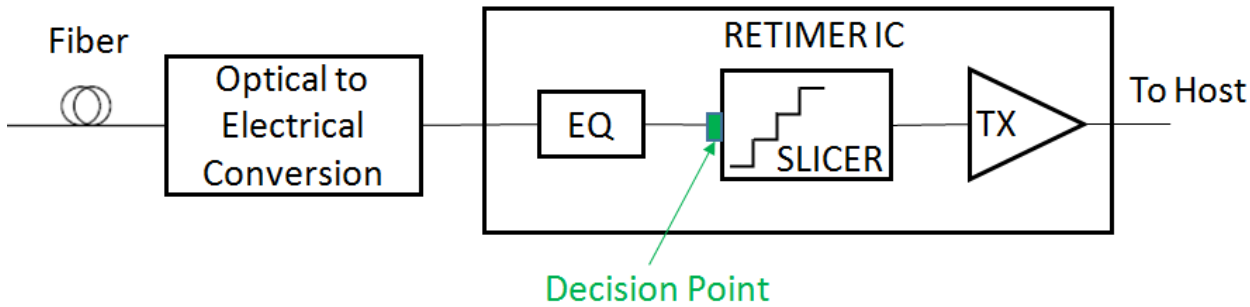

FIGURE 6-2: OPTICAL INGRESS PATH OF MODULE

Figure 6-3 is a view of the aggregate PAM4 data expressed as a histogram measured at a vertical slice in the center of the eye, showing the measurement method for SNR and level transition parameters.

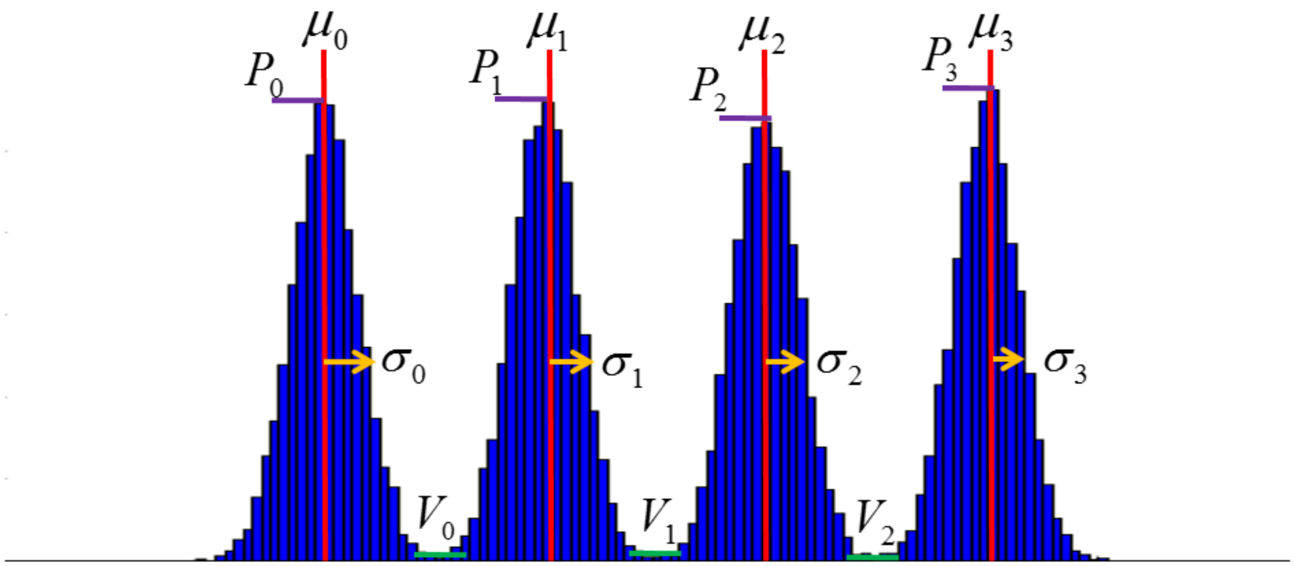

FIGURE 6-3: PAM4 VERTICAL SLICE HISTOGRAM

The histogram x-axis is in bins and the y-axis is in number of bin hits. The number of bins and the hit count magnitude is vendor specific. The histogram is taken at the point in the time domain where data is converted from analog to digital. The PAM4 slicer determines the best points to split the data between values of 0, 1, 2 or 3. The peak is the bin with the largest number of counts between any two valleys (or below valley 1/above valley 3 for the first and last peaks). The valley location is determined by the slicer, and is the bin number where data below is considered to be i and data above is considered to be i+1.

The calculations for the reported eye parameters are:

SNR = $10 * \log_{10}(\min\{SNR_0, SNR_1, SNR_2\})$ where $SNR_i = (\mu_{i+1} - \mu_i)/(\sigma_{i+1} + \sigma_i)$, expressed in 1/256 dB units

LTP = $10 * \log_{10}(\min\{LTP_0, LTP_1, LTP_2\})$ where $LTP_i = (P_{i+1} + P_i)/(2V_i)$, expressed in 1/256 dB units

Where,

μ_i: level of ith peak, optionally averaged over neighboring bins
σ_i: std dev of ith peak, optionally averaged over neighboring bins

P_i: height of ith peak, optionally averaged over neighboring bins

V_i: height of ith valley, optionally averaged over neighboring bins

For the vendor specified wavelength, the accuracy of the reported SNR and LTP parameters shall be better than +/-3 dB over specified temperature and voltage.

6.7.4 Detailed Description of New Monitored Parameters for PAM4

6.7.4.1 SNR

This feature measures the electrical signal-to-noise ratio on the ingress optical channel, as defined in Figure 6-3. It is the minimum of the individual eye SNR values, where the SNRi for each of the three eyes is defined as the ratio of the difference of the mean voltage between neighboring levels divided by the sum of the standard deviations of the two neighboring levels.

SNR is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example a value of 1380h will be interpreted as an SNR of 19.5 dB.

6.7.4.2 Residual ISI/Dispersion:

Chromatic dispersion is monitored at TP3 and will report the same value as an external dispersion meter (e.g., an optical vector analyzer) would report. The units are 0.1 ps/nm. For the vendor specified wavelength and line width, the accuracy of the reported Residual ISI/Dispersion parameter shall be better than +/-100 ps/nm over specified temperature and voltage.

6.7.4.3 PAM Level Transition Parameter

This feature measures the electrical level slicer noise, as defined in Figure 6-3. It is the minimum of the individual PAM level LTP values, where the LTP for each PAM level is defined as the average of the peak histogram intensity of neighboring PAM levels divided by the minimum histogram intensity between them. Both the SNR and LTP parameters measure signal-to-noise but the LTP parameter is more sensitive to a noise floor.

PAM Level Transition Parameter is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example a value of 3080h will be interpreted as an LTP of 48.5 dB. It is possible that the minimum histogram intensity between PAM levels is actually zero in which case this parameter would be infinite. In this case the special value of FFFFh will be used. If the parameter measures a value of greater than 255.996 dB but is not infinite, then FFFEh will be used.

6.7.4.4 Error Figures

Frame error rate is reported in RS(544,514) FEC equivalent frames (see IEEE 802.3 Clause 91.5). If the actual FEC is not RS(544,514) then the measured frame error rate is converted. So for example, if the FEC frame size is 10% larger than the RS(544,514) FEC frame, then the reported frame error rate will be 10% higher than the measured frame error rate. This is done so as to be able to compare frame error rates regardless of the FEC encoding employed.

Two different error figures may be supported:

- RS(544,514) Frame Error Rate (FER): This parameter measures the

uncorrected/errored RS(544,514) equivalent frames per second.
- Pre-FEC Bit Error Ratio (BER): This is the total number of errored bits that were corrected by the FEC during an interval divided by the total number of bits received in the interval. Note that different FEC schemes will have different maximum pre-FEC BER requirements for a specific corrected BER maximum target.

Both the BER and the FER will be monitored using the following technique:

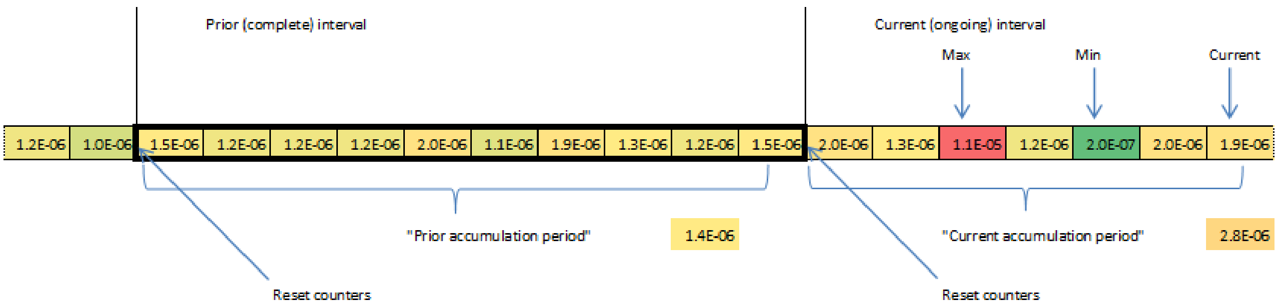

FIGURE 6-4: ERROR RATE ACCUMULATION INTERVALS

The module shall collect BER/FER data over a vendor-specific fine time slice, defined by the module (for example, 1 ms). The host may read the data at a slower rate.

The module calculates a BER/FER at each fine interval (light borders). The Host may have performance monitoring intervals (dark borders). Figure 6-4 shows a series (in time) of fine intervals punctuated by counter reset events that demark the host monitoring interval. If supported by the module, the host can read various calculated values. The selection of the which value(s) is/are available depends on the parameter type identifier (see Table 6-45).

Current:

If supported, the module shall keep a recent reading for the host to read at any time. This is referred to as the “instantaneous” value. For this value, a parameter type (See Table 6-45) of 12 for BER or 15 for FER is used.

Average:

If supported by the module, the average value shall be determined by using the counters reset function to program the averaging time interval. The module shall report a continuously averaged reading over the entire averaging interval. For this value, a parameter type of 4 for BER or 5 for FER is used. This value provides a glimpse as to how the current monitoring interval is performing. The module shall reset the counters for this purpose upon a write of 1b to register 250, bit 7 on page 20h.

Prior Period:

This value is the total averaged in the last monitoring interval as defined by the two most recent counter reset events. This is provided to assure that an interval can be calculated regardless of how quickly the host is reading the data.

If supported, the module shall allow the host to continue to read the BER/FER that was averaged between the last two counter reset events (i.e. between the two dark lines in Figure 6-4). For this value, a parameter type of 12 for BER and 16 for FER is used. The module shall reset the counters for this purpose upon a write of 1b to register 250, bit 7 on page 20h.

Latched Maximum/Maximum:

This is the largest/smallest fine-interval calculation since the last time the host read the data. The host can then keep track of the maximum of these readings to report as an overall maximum/minimum within its performance monitoring interval.

If supported, the module shall latch the lowest and highest (respectively) measurements it has calculated over any fine interval since the last time the host read each value. The module shall clear the corresponding latch when the host reads the value. These values are not cleared with the counters reset feature. For these values, a parameter type of 9 for BER minimum, 10 for BER maximum, 13 for FER minimum, and 15 for FER maximum is used.

Note that the thresholds system is maintained for BER and FER, but the low thresholds should be 0, and the high threshold for FER should also be 0 unless other error correcting schemes are present.

The error parameters will be interpreted as an unsigned 16-bit floating point number with 5 bits for base-10 exponent, offset by -24, and 11 bits for mantissa. Thus the format is:

$$m * 10^{s+o}$$

Where m ranges from 0 to 2047 (11 bits), s ranges from 0 to 31 (5 bits) and o is fixed at -24. The smallest non-zero number is m=1 and s=0 or 1*10^(-24). The largest number supported is m=2047 and s=31, or 2.047*10^10. Within the 2 bytes of the value (stored lowest byte first), m and s are encoded as follows:

TABLE 6-50 ENCODING FOR BER/FER

Byte	Bits	Description
1	7:3	Exponent (s)
1	2:0	Mantissa (m), bits 10:8
2	7:0	Mantissa (m), bits 7:0

6.7.5 Detailed Description of New Monitored Parameters for DWDM

6.7.5.1 TC Current

If supported, this parameter monitors the amount of current flowing to the TC of a cooled laser.

It is a 16-bit signed 2s complement value in increments of 0.1 mA. Thus the total range is from -3.2768 A to +3.2767 A.

6.7.5.2 Laser Frequency

If supported, this parameter monitors the difference (in frequency units) between the target center frequency and the actual current center frequency. It is a similar measurement to the Laser Temperature except expressed as a frequency difference instead of a temperature difference, and vendors may support one or the other measurement, or both.

It is a 16-bit signed 2s complement value in increments of 10 MHz. Thus the total range is from -327.68 GHz to 327.67 GHz.

6.7.5.3 Laser Temperature

If supported, this parameter monitors the laser temperature difference between the target laser temperature for a cooled laser, and the actual current temperature. It is a similar measurement to the Frequency Error except expressed as a temperature difference instead of a frequency difference, and vendors may support one or the other measurement, or both.

It is a 16-bit signed 2s complement value in increments of 1/256 ˚C. Thus the total range is from -128 ˚C to +128 ˚C.

A. Annex A

Editor's Note:For consideration as replacement text for subsection 6.2.7. Rate Select or as a stand-alone Annex. This proposed text is intended to clarify the rate select behavior without changing what is already documented. Please review carefully and provide comments on whether to keep this as a stand-alone Annex.

A.1 Rate Select and Configuration for Multi-rate Modules

The host system (fixed-side) can use the management interface to reconfigure modules (free-side) to operate at different data rates or to comply with different specifications. One method of reconfiguration is for the host to write directly, one at a time, to the various controls provided by the module. Alternatively the module may offer optional rate select controls whereby the host writes to a single location and the module firmware makes all necessary adjustments to change operation from one rate to another.

When rate select controls are provided, the module may automatically make changes to the Tx and Rx datapath components, including the ability to:

- Enable/Disable (bypass) Tx and Rx CDRs
- Enable/Disable/Adjust Tx input equalizers and set fixed or adaptive modes of operation
- Enable/Disable/Adjust Rx output emphasis and Rx output amplitude
- Adjust the bandwidth and/or gain of internal components

Various advertising bits state which optional features are implemented by a module. Key bits for this discussion are:

<u>CDR options</u>
Page 00h, byte 129, bits 3-2: CDRs implemented
Page 00h, byte 194, bits 7-6: CDR On/Off Control implemented

<u>Tx Input Equalizer options</u>
Page 00h, byte 193, bit 3: Tx Input Equalizer Auto Adaptive Capable
Page 00h, byte 193, bit 2: Tx Input Equalizer Fixed Programmable Settings
Page 03h, byte 224, bits 7-4: Tx Input Equalizer Maximum Magnitude Supported

<u>Rx Output Emphasis options</u>
Page 00h, byte 193, bit 1: Rx Output Emphasis Control implemented
Page 03h, byte 224, bits 3-0: Rx Output Emphasis Maximum Magnitude Supported
Page 03h, byte 225, bits 5-4: Rx Output Emphasis Type

<u>Rx Output Amplitude options</u>
Page 00h, byte 193, bit 0: Rx Output Amplitude Control implemented
Page 03h, byte 225, bits 3-0: Rx Output Amplitude Codes Supported

<u>Rate Select options</u>
Page 00h, byte 195, bit 5: Rate Select implemented
Page 00h, byte 221, bits 3-2: Rate Selection Type Declaration
Page 00h, byte 141, bits 1-0: Extended Rate Selection Compliance Tags

A.1.1 Direct Control Configuration

The host system can directly control the CDRs, Tx Input Equalizers, Rx Output Emphasis and Rx Output Amplitude if those options are implemented by the module. After checking the various advertising bits, the host can control these features using the control bits at:

Page 00h, byte 98: Tx and Rx CDR control bits
Page 03h, bytes 234-235: Tx Input Equalizer settings
Page 03h, byte 241, bits 3-0: Tx Input Adaptive Equalizer enable bits
Page 03h, bytes 236-237: Rx Output Emphasis settings
Page 03h, bytes 238-239: Rx Output Amplitude settings

Note that CDRs and Tx input equalizers are designed for operation at the maximum data rate specified for the module. For module operation at low data rates, the host may need to disable Tx and Rx CDRs and set the Tx input equalizers for 0 dB of equalization.

A.1.1.1 Rate Select

If rate select is supported by a module, the host can control data rates using either the Tx & Rx rate select control bits (bytes 87-88) or using the Tx & Rx application select control bits (bytes 89-92 and 94-97). There are several advertising bits that tell the host whether the module supports rate select, and which types of rate select are available.

Table A-1 summarizes the advertising bits related to Rate Select support.

TABLE A-1 RATE SELECT ADVERTISING BITS

Field	RS supported	RS Type		Ext RS Compliance		
Page	**00h**					
Byte	**195**	**221**		**141**		
Bit	**5**	**3**	**2**	**1**	**0**	**Meaning**
Value	0	X	X	X	X	Rate select not supported. Use manual controls if available.
	1	0	0	X	X	Reserved
		1	1	X	X	Reserved
		1	0	0	0	Reserved
				1	1	Reserved
				0	1	Extended Rate Select Version 1 supported.
				1	0	Extended Rate Select Version 2 supported.
		0	1	X	X	Rate selection using Application Select Table supported.

If the module supports rate select the host can change configuration by using the rate select or application select controls at:

Page 00h, bytes 87-88: Tx and Rx Rate Select control bits
Or
Page 00h, bytes 89-92: Rx Application Select control bits
Page 00h, bytes 94-97: Tx Application Select control bits

The module is responsible for making all necessary adjustments for operation at the selected data rate and/or application code. These adjustments may include changes to Tx and Rx bandwidths, changes in CDR operation, and adjustments to equalizer, emphasis and amplitude settings, without requiring the host to write those control bits.

If the module makes adjustments to these settings there is no requirement for the module firmware to change the related control bits. For example, if the module bypasses the Tx or Rx CDRs in order to operate at a reduced data rate, byte 98 may still be set to show the CDRs enabled.

A.1.1.2 Extended Rate Selection

If one of the extended rate select versions is supported, as listed in Table A-2, then the host can use bytes 87-88 to optimize the Tx and Rx data paths for particular data rates. Two bits are assigned to each receiver in Byte 87 (Rxn_Rate_Select) and two bits for each transmitter in Byte 88 (Txn_Rate_Select) to specify up to four bit rates.

TABLE A-2 XN_RATE_SELECT WITH EXTENDED RATE SELECTION

xN_Rate_Select		Description
MSB	LSB	
Version 1 - Page 00h Byte 141 Bit 0 = 1		
0	0	Optimized for bit rates less than 2.2 Gbps
0	1	Optimized for bit rates from 2.2 up to 6.6 Gbps
1	0	Optimized for 6.6 Gbps bit rates and above
1	1	Reserved
Version 2 - Page 00h Byte 141 Bit 1 = 1		
0	0	Optimized for bit rates less than 12 Gbps
0	1	Optimized for bit rates from 12 up to 24 Gbps
1	0	Optimized for bit rates from 24 up to 26 Gbps
1	1	Optimized for 26 Gbps bit rates and above

A.1.1.3 Rate Selection Using Application Select Table

If rate selection using Application Select Table is supported, as listed in Table A-1, then the host can use bytes 89-92 to select the application for the Rx path and bytes 94-97 to select the application for the Tx path. The host reads the entire Application Select Table at Page 01h to determine the capabilities of the module. The host controls each channel separately by writing the Control Mode and Table Select (TS) fields to Bytes 89-92 and Bytes 94-97. The format for these bytes is shown in Table A-3.

TABLE A-3 APPLICATION SELECT (PAGE 00H BYTES 89-92 AND BYTES 94-97)

7	6	5	4	3	2	1	0
Control Mode		Table Select TS					

Control Mode defines the application control mode as listed in Table A-4. Table Select selects the free side device behavior from the AST among 63 possibilities (000000 to 111110). Note that (111111) is invalid.

TABLE A-4 CONTROL MODE DEFINITION

Bit 7	Bit 6	Function	Bytes 87-88 Control	Table Select Control
0	0	Extended rate selection	LSB and MSB are used according to declaration bits.	Ignored
1	Don't care	Application select	Ignored	field points to application

Note: Default values for control mode is 00 and is volatile memory.

-----------------END OF DOCUMENT-----------------